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| *Title:* | **Fast Intra SDC coding for 3D-HEVC Intra Coding** | | | |
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| *Purpose:* | Proposal | | | |
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# Abstract

In current High Efficiency Video Coding (HEVC)-based depth intra coding, a full RD search list is created and both non-SDC coding and SDC coding are tested for full-RD cost calculation. To speedup the depth intra coding, we propose to test SDC coding for selected candidates modes based on the non-SDC RD cost of each mode. Two methods are proposed. Experiment results show that the proposed methd1 achieves more than 15% All Intra encoding time saving with negligible BD-rate change and method2 achieves more than 10% All Intra encoding time saving with small BD-rate gain under CTC.

# Introduction

In current 3D-HEVC depth intra coding, the Segment-wise DC Coding (SDC) approach provides an alternative residual coding method. With SDC, the residual data (one or two constant residual values within one PU) is coded without transform and quantization processes. Whether SDC is used is signalled in the coding unit parameters structure at PU level. The partition size of CU containing a SDC coded PU is always 2Nx2N. SDC can be applied to all depth intra prediction modes including HEVC intra prediction modes and depth modelling modes. For HEVC intra prediction modes, the entire PU is considered as one segment, while for DMM modes, there are two segments. [1]

However, not all depth intra prediction modes (including HEVC intra prediction modes and depth modelling modes) need to test SDC for full-RD cost calculation. Since SDC is a supplementary mode based on intra prediction modes, it makes sense to just test SDC for intra prediction modes with small RD cost rather than all the intra prediction modes.

# Proposed solution

In this proposal, we selectively skip intra SDC full RD cost calculation based on the non-SDC RD cost of each candidate mode. Basically, we notice the modes with small full-RD cost when SDC is disabled are also very likely to have small full-RD cost when SDC is enabled. Therefore, we use the mode with smallest full-RD cost when SDC is disabled, **Non\_SDC\_Mode1**, as one of the indicators for SDC full RD cost calculation skip decision.

**2.1 Method1**

Our proposed method1 is summarized in Figure 1. Here, **Non\_SDC\_Mode1** is mode with smallest full-RD cost when SDC is disabled; **Non\_SDC\_Mode2** is mode with second smallest full-RD cost when SDC is disabled; **Non\_SDC\_Mode3** is mode with third smallest full-RD cost when SDC is disabled. **Best\_Mode** is mode with smallest full-RD cost and **Cost(Best\_Mode)** is the full RD cost value of **Best\_Mode**. Both **Best\_Mode** and **Cost(Best\_Mode)** will be updated during RDO loop. The variance threshold, **varThreshold1**, in Figure 1 is set to 1.



Figure 1. Flow chart of proposed fast SDC mode selection method1 for intra depth map coding

**2.1 Method2**

We show Method 2 in Figure 2. We replace the condition “**Mode(i)** is not the first mode in full-RD cost calculation list” in Method 1 with condition “PU variance is smaller than varThreshold2, where **varThreshold2** = 4.



Figure 2. Flow chart of proposed fast SDC mode selection method2 for intra depth map coding

# Experimental results

The proposed method is implemented on top of HTM-11.0, and simulations were performed under both All Intra configuration and CTC [2].

The results of method1 are summarized in Table 1 and Table 2. More than 15% All Intra encoding time saving is achieved with negligible BD-rate change.

**3.1 Result of Mehod1**

Table 1: BD rate results for 3-view case under All Intra Condition



Table 2: BD rate results for 3-view case under CTC



The results of method1 are summarized in Table 3 and Table 4. More than 10% All Intra encoding time saving is achieved without noticeable BD-rate change.

**3.2 Result of Mehod2**

Table 3: BD rate results for 3-view case under All Intra Condition



Table 4: BD rate results for 3-view case under CTC



# References

1. G. Tech, K. Wegner, Y. Chen, S. Yea “Test Model 8 of 3D-HEVC and MV-HEVC” in JCT3V-H1003, Valencia Spain, 29 Mar. – 4 Apr. 2014
2. K. Müller, A. Vetro, “Common Test Conditions of 3DV Core Experiments,” JCT3V-G1100, San Jose, USA, January 2014.

# Patent rights declaration(s)

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