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| *Title:* | Tile-Level Rate Control for Multi-core Platform on HM | | |
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# Abstract

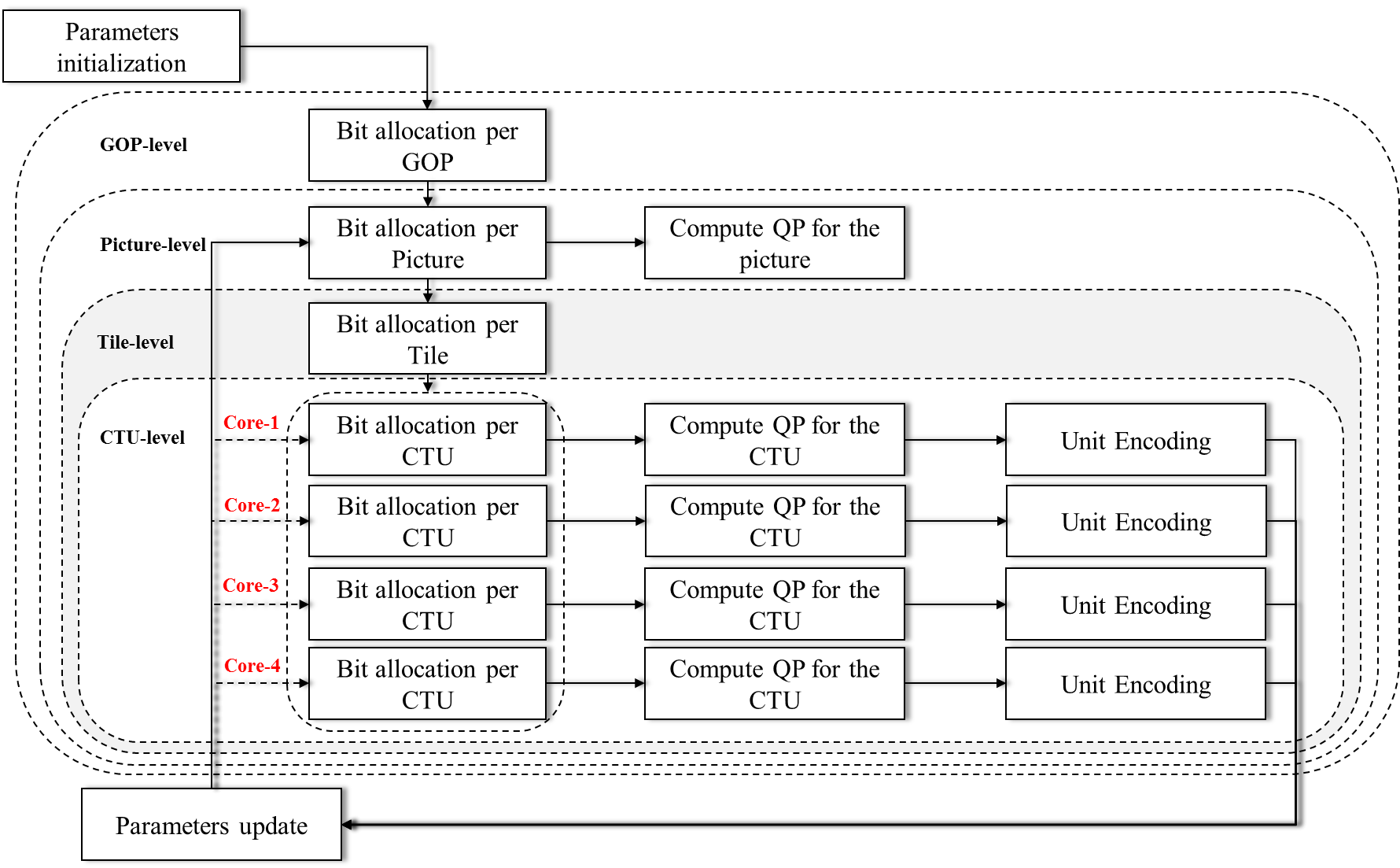
This contribution proposes a tile level rate control for multi-core platform on HEVC. The proposed tile-level rate control algorithm is integrated on HM-16.12. This contribution is proposed to favor multi-core platform in tile-level. The proposed algorithm is evaluated with three different tile configurations (4, 6, and 8 tile partitions). Compared with the existing rate control algorithm in HM-16.12 (without tile-level rate control as an anchor), the proposed algorithm yields similar Y PSNR and BD-rate performance. The bitrate accuracy is also slightly improved for all tile configuration tests.

# Introduction

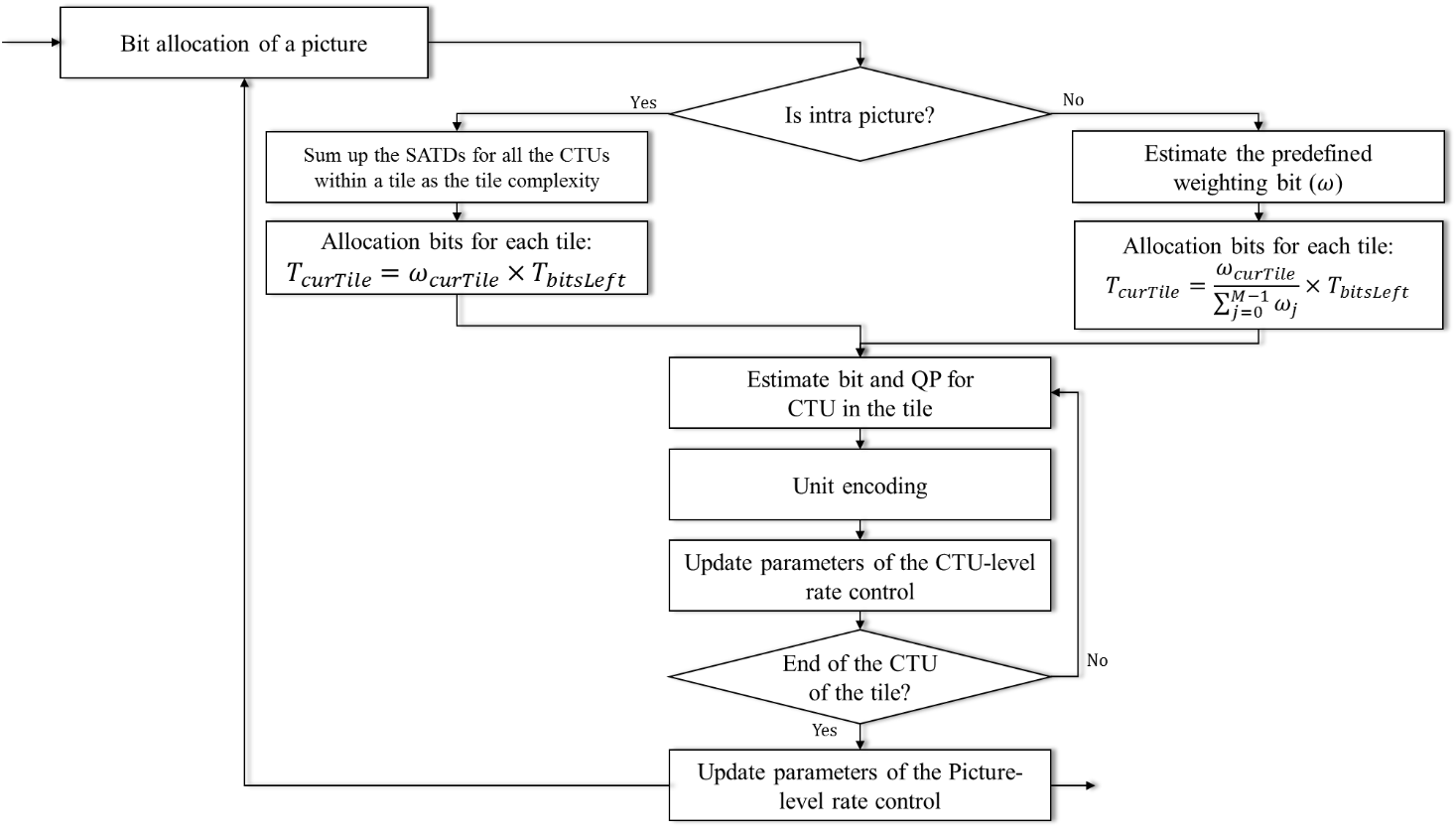
The idea of Tile-level rate control for HEVC was introduced and suggested as a further study contribution [1] in the 22nd JCT-VC meeting, Geneva. It is proposed due to tile parallelism is practically more considerable for a fast encoding and decoding of video technology. However, tile parallelism will lose BD-rate performance with number partition of tiles. It is due to there exists what so-called with dependency breaking along partition boundaries. In tile-level multi-core case, all the tiles are independently encoded and their QP must be independently determined as well. Thus, it is not easy to meet the rate constraint and also realize the desired visual quality. In addition, none of the major rate control models developed in the video coding standards provides any consideration for tile-level parallelism cases. Accordingly, to maximize compression performance (i.e., better coding efficiency and/or better visual quality), it is important to control the encoding processes for each tile.

# Proposed techniques

Broadly, rate control algorithms are designed primarily with multi-level bit allocations that consider only group-of-picture (GOP)-, picture-, and block-unit levels. The proposed contribution embeds a tile-level bit allocation to favor tile-level parallelism, as shown in Figure 1. The proposed algorithm is organized based on the R-Lambda model rate control of HM 16.12. There is no any changing of the rate control for GOP-, picture-, and CTU-levels. Once rate control in tile-level is performed, all CTUs in each tile will be coded with the CTU-level rate control. Then, all rate control parameters such as *α* and *β* will be updated using the average values from all the tile partitions after encoding process.



**Figure 1. Block-diagram of the proposed tile-level rate control algorithm**

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**Figure 2. Bit allocation flowchart of the proposed tile-level rate control algorithm**

Figure 2 illustrates how the proposed algorithm allocates some bits for a tile in intra and inter picture. For tile in intra picture, we consider sum of SATD values of all CTUs in tile as tile complexity. We found high correlation between tile SATD values and actual bits of the tiles. Thus, appropriate bits are adaptively allocated for each tile partition according to its complexity. For inter pictures, tile-level bit allocation organizes bits for the tiles based on a weight ratio of the bits derived at the picture level. In addition, we also employ the actual generated bit of collocated tiles in the recently coded pictures (under random access configuration) when allocating bits for the current tile of the inter pictures.

In the R-lambda based rate control model, lambda is estimated by:

|  |  |
| --- | --- |
|  | (1) |

Assume that the target number of bits for current picture is . Thus, the Tile-level bit allocation  should satisfy

|  |  |
| --- | --- |
|  | (2) |

1. **Tile-level bit allocation for tile in Intra Picture**

As we mentioned earlier that bit allocation for tiles in intra picture is determined adaptively according to the complexity content of tile. The SATD value of all the CTUs in a tile is taken into consideration to measure the tile complexity. Thus, is expressed as:

|  |  |
| --- | --- |
|  | (3) |

is priory calculated from the target bit of picture and the bit header (included bit of slice header) subtraction. is a complexity ratio, defined as:

|  |  |
| --- | --- |
|  | (4) |
|  | (5) |

where denotes the current tile complexity, is the total number of tiles in a picture, *N* denotes the total number of CTUs in -th tile, and is the SATD value of -th CTU. Note that the SATD for each CTU is computed during the picture-level rate control. Thus, there is no extra computational load associated with estimating the target bit in the tile-level of the intra picture

1. **Tile-level bit allocation for tile in Inter Picture**

For tile in inter picture, is designed with hierarchical–B coding structure under random access configuration. is determined using the inverse form of Eq. (1) according to total number of pixels in tile, information derived from the picture-level, such as as , and , and actual bits of the collocated tiles of reference pictures, . We regarded all these factors as a weight bit to appropriately assign bits for tiles in inter pictures. Thus, can be expressed as:

|  |  |
| --- | --- |
|  | (6) |
|  | (7) |

where denotes the actual bit of collocated tile of previous picture, is the weighted bits of the -th tile in a picture, is the total number of pixels in the current tile, and , , and are the λ and rate control parameters from the picture level, respectively.

1. **Updating the rate control parameters**

In general, rate control parameters and are updated after encoding all the CTUs in a picture. We note that in HM-16.12 all the CTUs are coded in raster scan order within a picture. Along with the proposed tile-level rate control, the CTU-level rate control runs with information from the corresponding tile. All the rate control parameters in the CTU-level are also updated. With respect to the picture level, all the rate control parameters are updated using the average values from all the tile partitions.

# Experimental results

The experiments are performed based on HM-16.12, and the common test conditions specified in [2] are followed. The rate control used in the HM-16.12 without tile-level rate control is enabled as an anchor for the evaluation. We used three different tile partitions (4, 6 and 8 tile partitions) with non-uniform mode. All experiments were conducted under ‘Random Access’ and ‘Low Delay B’ configurations.

Table 1 and Table 2 tabulate coding efficiency performance of the proposed tile-level rate control against the anchor. The summary results on rate control accuracy when targeting the HM anchor bitrate are provided in Table 3. The Class D sequences are excluded in the experiments due to those sequences cannot support our tile partition configurations.

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| **Table 1** R-D performance of the proposed Tile-level rate control algorithm (Random Access) | | | | | | | | | | | | |
|  | | | **4-Tiles** | | | **6-Tiles** | | | | **8-Tiles** | | |
| **Y** | **U** | **V** | **Y** | **U** | **V** | | **Y** | **U** | **V** |
| Class A | | | -0.1% | -2.5% | -0.7% | -0.1% | 1.1% | 1.7% | | -0.1% | -1.1% | -0.3% |
| Class B | | | -4.4% | -3.5% | -2.7% | -4.4% | -4.5% | -3.9% | | -4.1% | -3.8% | -3.7% |
| Class C | | | -2.5% | -1.5% | -1.0% | -2.5% | -1.6% | -0.7% | | -2.4% | -1.2% | -0.4% |
| Class D | | |  |  |  |  |  |  | |  |  |  |
| Class E | | |  |  |  |  |  |  | |  |  |  |
| Class F | | | 1.4% | 3.3% | 3.2% | -1.8% | 2.5% | 3.3% | | 0.3% | 2.3% | 2.7% |
| **Overall**  **without Class F** | **BD-rate** | | **-2.5%** | **-2.6%** | **-1.6%** | **-2.8%** | **-1.9%** | **-1.2%** | | **-2.4%** | **-2.2%** | **-0.4%** |
| **Enc. Time** | | **106%** | | | **104%** | | | | **102%** | | |
| Overall  with Class F | BD-rate | | -1.6% | -1.2% | -0.4% | -1.8% | -1.9% | -1.2% | | -1.8% | -0.8% | -0.4% |
| Enc. Time | | 105% | | | 103% | | | | 102% | | |
|  |  | |  |  |  |  |  |  | |  |  |  |
|  |  | |  |  |  |  |  |  | |  |  |  |
|  | | **Table 2** R-D performance of the proposed Tile-level rate control algorithm (Low-Delay B) | | | | | | | | | | |
|  | | | **4-Tiles** | | | **6-Tiles** | | | | **8-Tiles** | | |
| **Y** | **U** | **V** | **Y** | **U** | **V** | | **Y** | **U** | **V** |
| Class A | | |  |  |  |  |  |  | |  |  |  |
| Class B | | | -1.7% | 0.5% | 0.9% | -1.6% | 0.5% | 0.9% | | -2.3% | -0.5% | -0.5% |
| Class C | | | -0.3% | 1.9% | 1.5% | -0.3% | 1.9% | 1.5% | | -0.2% | 1.4% | 2.1% |
| Class D | | |  |  |  |  |  |  | |  |  |  |
| Class E | | | 2.4% | 8.0% | 7.9% | -1.6% | -1.7% | -2.4% | | 2.2% | 6.9% | 7.1% |
| Class F | | | -1.3% | 3.0% | 5.5% | -1.1% | 1.9% | 4.8% | | -0.5% | 1.0% | 4.6% |
| **Overall**  **without Class F** | **BD-rate** | | **0.2%** | **2.9%** | **2.9%** | **-1.2%** | **0.5%** | **0.3%** | | **-0.5%** | **2.1%** | **2.2%** |
| **Enc. Time** | | 100% | | | 105% | | | | 104% | | |
| Overall  with Class F | BD-rate | | -0.5% | 2.9% | 3.5% | -1.2% | 0.8% | | 1.4% | -0.5% | 1.7% | 2.8% |
| Enc. Time | | 100% | | | 104% | | | | 104% | | |

**Table 3** Rate control accuracy of the proposed Tile-level rate control algorithm

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Test case/**  **Tile partition** | **Sequence** | **Average of bitrate accuracy** | | **Delta bitrate accuracy** | **Y-PSNR improvement** |
| **RC in HM-16.12 without tile-level RC** | **Proposed tile-level RC** |
| RA-Main/  4 Tiles | Class A | 0.54% | 0.73% | 0.19% | 0.00 dB |
| Class B | 0.78% | 1.05% | 0.27% | 0.12 dB |
| Class C | 0.36% | 0.60% | 0.23% | 0.11 dB |
| **Average** | | **0.59%** | **0.82%** | **0.23%** | **0.08 dB** |
| RA-Main/  6 Tiles | Class A | 0.56% | 0.73% | 0.17% | 0.01 dB |
| Class B | 0.79% | 1.06% | 0.27% | 0.12 dB |
| Class C | 0.36% | 0.61% | 0.25% | 0.11 dB |
| **Average** | | **0.59%** | **0.82%** | **0.23%** | **0.09 dB** |
| RA-Main/  8 Tiles | Class A | 0.55% | 0.75% | 0.20% | 0.02 dB |
| Class B | 0.78% | 1.07% | 0.29% | 0.12 dB |
| Class C | 0.36% | 0.61% | 0.25% | 0.11 dB |
| **Average** | | **0.58%** | **0.83%** | **0.25%** | **0.08 dB** |
| LB-Main/  4 Tiles | Class B | 0.06% | 0.12% | 0.06% | 0.03 dB |
| Class C | 0.15% | 0.18% | 0.04% | 0.02 dB |
| Class E | 0.24% | 0.28% | 0.03% | -0.05 dB |
| **Average** | | **0.10%** | **0.15%** | **0.04%** | **0.03 dB** |
| LB-Main/  6 Tiles | Class B | 0.07% | 0.13% | 0.03% | 0.05 dB |
| Class C | 0.15% | 0.18% | 0.02% | 0.01 dB |
| Class E | 0.66% | 0.66% | 0.06% | 0.06 dB |
| **Average** | | **0.24%** | **0.28%** | **0.04%** | **0.03 dB** |
| LB-Main/  8 Tiles | Class B | 0.07% | 0.13% | 0.06% | 0.05 dB |
| Class C | 0.15% | 0.18% | 0.03% | 0.01 dB |
| Class E | 0.24% | 0.29% | 0.03% | -0.05 dB |
| **Average** | | **0.10%** | **0.15%** | **0.05%** | **0.03 dB** |

# Conclusion

This contribution proposes a tile-level bit allocation of rate control to favor multi-core platform in HM. It is reported that the proposed tile-level rate control model can achieve coding gain, visual quality, and bitrate accuracy improvements in both low-delay and random-access configurations with negligible encoding time increased.

# References

1. I. Marzuki, Y. Ahn, W. Lim, and D. Sim, “Tile-level rate control for multi-core platform,” JCTVC-V0088, 22nd JCT-VC meeting, Geneva, CH, Oct. 2015.
2. F. Bossen, “Common HM test conditions and software reference configurations,” JCTVC-L1100, 12th JCT-VC meeting, Geneva, CH, Jan. 2013.

# Patent rights declaration(s)

**KWU may have current or pending patent rights relating to the technology described in this contribution and, conditioned on reciprocity, is prepared to grant licenses under reasonable and non-discriminatory terms as necessary for implementation of the resulting ITU-T Recommendation | ISO/IEC International Standard (per box 2 of the ITU-T/ITU-R/ISO/IEC patent statement and licensing declaration form).**