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| **Joint Collaborative Team on Video Coding (JCT-VC)**  **of ITU-T SG 16 WP 3 and ISO/IEC JTC 1/SC 29/WG 11**  16th Meeting: San José, US, 9–17 Jan. 2014 | Document: JCTVC-P0289 |

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| *Title:* | **Non-RCE1: Combination of subtests A1 and B3.a of RCE1** | | |
| *Status:* | Input Document to JCT-VC | | |
| *Purpose:* | Proposal | | |
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# Abstract

This document reports a combination of subtests A1 and B3a of HEVC Range Extensions core experiment 1. In this combination, as proposed in subtest A1, the coding of *coeff\_abs\_level\_greater1* and *coeff\_abs\_level\_greater2* flags is skipped for the current 4×4 subblock if the Golomb Rice parameter at the end of the previous 4×4 subblock is greater than or equal to a threshold. In addition, as proposed in subtest B3a, alignment of the ivlCurrRange to 256 is performed depending on the condition that some escape data (*coeff\_abs\_level\_remaining*) is present in the current 4×4 subblock

It is asserted that compared to subtest A1, the combination more tightly bounds the number of bins coded using bypass CABAC mode for each 4×4 subblock. It is also reported that under AHG18 test conditions, the average bin count reduction for intra 16-bit and lowdelay 16-bit configurations is 18% and 11%, respectively.

# Introduction

This document reports a combination of subtests A1 and B3a of HEVC Range Extensions core experiment 1 (RCE1). In this combination, the coding of *coeff\_abs\_level\_greater1* and *coeff\_abs\_level\_greater2* flags is skipped for the current 4×4 subblock if the Golomb Rice parameter at the end of the previous 4×4 subblock is greater than or equal to a threshold. In addition, as proposed in subtest B3a, alignment of the ivlCurrRange to 256 is performed depending on the condition that some escape data (*coeff\_abs\_level\_remaining*) is present in the current 4×4 subblock.

# Simulation results

The proposal is implemented on top of HM12.1\_Rext5.1. Simulations are performed under AHG18, AHG5 and AHG8 (lossless) test conditions. The performance is compared to the anchor in terms of BD-rate savings.

## AHG18 results



Table 1: BD-rate results for the proposed combination of subtests A1 and B3a under AHG18 test conditions (threshold 4)



Table : BD-rate results for the proposed combination of subtests A1 and B3a under AHG8 test conditions (threshold 4)



Table : BD-rate results for the proposed combination of subtests A1 and B3a under AHG5 test conditions (threshold 4)

# Average Bin counts

Table 4 presents the average bin counts for AHG18 test conditions. It can be seen that for 16-bit test conditions, the average bin count reduction for intra and lowdelay configurations is 18% and 11%, respectively.



Table : Average bin counts for the proposed combination of subtests A1 and B3a under AHG5 test conditions (threshold 4)

# Worst-case complexity analysis

|  |  |  |  |
| --- | --- | --- | --- |
|  | Total number of context bins | Total number of bypass bins with CABAC | Total number of bypass bins (raw) |
| Base | 16+8+1 = 25 | (1+46) + (1+39)\*15 = 647 | 0 |
| *coeff\_abs\_level\_greaterX* bypass, no bypass alignment | 16 | 16 (sign flags) | 0 |
| No *coeff\_abs\_level\_greaterX* bypass + bypass alignment | 16+8+1 = 25 | 0 | (1+46) + (1+39)\*15 = 647 |
| *coeff\_abs\_level\_greaterX* bypass + bypass alignment | 16 | 0 | (1+46) + (1+39)\*15 = 647 |

This assumes fast Golomb Rice parameter adaptation with a maximum of 7.

# Conclusions

We have proposed a combination of subtests A1 and B3a of HEVC Range Extensions core experiment 1. In this combination, as proposed in subtest A1, the coding of *coeff\_abs\_level\_greater1* and *coeff\_abs\_level\_greater2* flags is skipped for the current 4×4 subblock if the Golomb Rice parameter at the end of the previous 4×4 subblock is greater than or equal to a threshold. In addition, as proposed in subtest B3a, alignment of the ivlCurrRange to 256 is performed depending on the condition that some escape data (*coeff\_abs\_level\_remaining*) is present in the current 4×4 subblock.

Worst case complexity analysis indicates that the combination more tightly bounds the number of bins coded using bypass CABAC mode for each 4×4 subblock to 16. It is also reported that under AHG18 test conditions, the average bin count reduction for intra 16-bit and lowdelay 16-bit configurations is 18% and 11%, respectively.

# Patent rights declaration(s)

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