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| **Joint Collaborative Team on Video Coding (JCT-VC)**  **of ITU-T SG 16 WP 3 and ISO/IEC JTC 1/SC 29/WG 11**  15th Meeting: Geneva, CH, 23 Oct. – 1 Nov. 2013 | Document: JCTVC-O0115 |

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| *Title:* | **Pipeline and parallel architecture for the SHVC decoder** | | |
| *Status:* | Input Document to JCT-VC | | |
| *Purpose:* | Information | | |
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| *Source:* | [Name of sourcing organization, AHG, etc.] | | |

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# Abstract

This contribution provides a complete implementation of the SHVC decoder under the *GPAC* player. The SHVC decoder is based on the open source software *OpenHEVC*, which implements a conforming HEVC decoder. The proposed pipeline and parallel SHVC decoder enables two levels of parallelism. The first level decodes the base layer and the enhancement layer frames in parallel. The second level of parallelism performs the decoding of both the base layer and the enhancement layer in parallel through the HEVC high-level parallel processing solutions (wave-front and tile).

Experimental results carried out on a computer fitted with an Intel Xeon processor running at 3.4 GHz showed that the pipeline SHVC decoder achieves the decoding of 1920x1080 base layer and 2560x1600 enhancement layer at 45 frames per second when using six concurrent threads.

# Introduction

The scalable extension of the High Efficiency Video Coding (HEVC) is currently being defined jointly by the ITU-T Video Coding Experts Group and the ISO/IEC Moving Picture Experts Group [1]. At the 13th Meeting in Incheon, only the “reference index based” method was selected and implemented in the SHVC test model (SHM-3) [2]. In this contribution we provide a pipeline and parallel architecture for the “reference index based” SHVC decoder. The proposed real time SHVC decoder is based on the *OpenHEVC* software, which implements a conforming HEVC decoder.

In the case of spatial scalability with two layers (base layer and enhancement layer), the SHVC decoder uses two instances of the *OpenHEVC* decoder [3], one for each layer. The first *OpenHEVC* instance decodes the base layer frame and feeds the second instance with the decoded base layer (BL) frame and its motion vectors (MVs). The second *OpenHEVC* decoder first up-samples and scales the base layer picture and its MVs, respectively, and then decodes the enhancement layer (EL) frame with using the up-sampled base layer picture as an additional reference picture for inter-layer prediction.

The proposed pipeline and parallel SHVC architecture enables two levels of parallelism. The first level performs the decoding of the base layer and the enhancement layer frames simultaneously on separate threads. For the 1rst decoded frame, the EL decoder waits until the base layer frame has been decoded and then the EL frame *i* is simultaneously decoded with the next BL frame (frame *i+1*).

For each decoder, the second parallelism level enables the decoding of both base layer and the enhancement layer frames in parallel based on the HEVC high level parallel processing solutions. Moreover, the upsampling of the base layer and the scaling its MVs are also carried out in parallel. In fact, when parallel decoding of the EL frame is enabled, the CTB rows of the base layer picture and the corresponding MVs are also up-sampled and scaled in parallel.

On an Intel Xeon processor running at 3.6 GHz, the proposed pipeline and parallel SHVC architecture achieves a real time decoding of 1080p45 base layer and 1600p45 enhancement layer with using 6 concurrent threads.

# Experimental results

To assess the performance of the SHVC decoder, the HEVC test video sequences were encoded with SHVC reference software [4] in two spatial scalability configurations: x2 and x1.5. The SHVC video sequences were coded in low delay coding configuration, which is widely adopted in video streaming applications. The quantization parameter (QP) of the base layer was set to 27 and 32, while the QP of the enhancement layer is equal to the base layer QP minus 2. The number of threads used to decode the BL and the EL are noted n and m, respectively. In addition to the single thread configuration (m = n = 1), the number of threads in the pipeline SHVC architecture are the following (n, m) {(1, 1), (1, 2), (1, 3), (1, 4), (2, 4)}. Table 1 gives the average bitrate of the BL and EL for the considered video sequences.

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| Configurations | | BL bitrate (Kbps) | EL bitrate (Kbps) |
| QP | EL resolutions |
| 32 | 1920x1080 | 1645 | 3318 |
| 2560x1600 | 4908 | 11788 |
| 3840x2160 | 13615 | 34162 |
| 27 | 1920x1080 | 2961 | 9539 |
| 2560x1600 | 9249 | 24196 |
| 3840x2160 | 29754 | 80262 |

Tableau 1 – Average bitrate of the SHVC bitstream of the considered video sequences

Figure 1 illustrates the decoding time per frame versus the number of concurrent threads for the three main decoding steps, including the BL decoding, the up-sampling of the BL picture and the EL decoding. We can notice that the decoding time of the three steps remains constant with using one thread and two threads (two decoders in parallel). In these two configurations each step is performance on a single thread. However, the whole decoding time, in the later configuration, decreases by the BL decoding time since the decoding of the BL and the EL are performed in parallel in the pipeline architecture. For number of threads between 3 and 5, we only increases the number of threads for the EL, since the decoding time of the EL including the up-sampling of the BL is higher than the decoding time of the BL and the WPP solution is more efficient with large video resolutions.

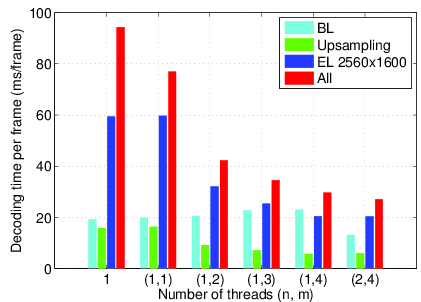


Figure 1 – Decoding time performance of the pipeline SHVC decoder

Figure 2 illustrates the decoding time performance of the pipeline SHVC decoder following the number of considered threads. The SHVC implementation reaches a real time decoding of EL resolution with 1600p45 and 2160p20 with using six concurrent threads.

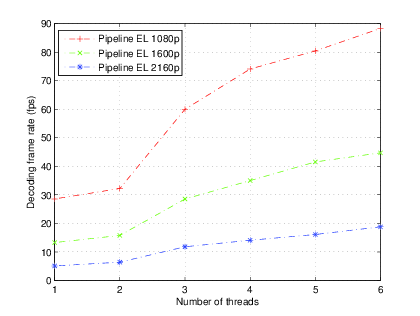


Figure 2 – Decoding frame rate performance of the Pipeline SHVC decoder

# Conclusion

In this contribution we provided a pipeline and parallel architecture for the SHVC decoder. This implementation enables two levels of parallelism by decoding the BL and EL frames on separate threads and the decoding of each layer in performed in parallel through the wavefront parallel processing solution.

The real time SHVC decoder is being integrated in the GPAC player [5] witch parses the MP4 fileformat and enabling to switch between tracks corresponding to the base layer and the enhancement layer.

# Acknowledgement

This work is part the European project Hybrid HEVC Broadcast Broadband Video Services (H2B2VS).

# References

1. J. Chen, J. Boyce, Y. Ye, Miska, and M. Hannuksela. Scalable high efficiency video coding test model 3 (SHM 3). In document JCTVC-N1007. 14th Meeting: Vienna, Austria, July 2013.
2. J. Chen, J. Boyce, Y. Yan and M. M. Hannuksela, “Scalable High Efficiency Video Coding Draft 3”, JCTVC-N1008, 14th JCTVC Meeting Vienna, AT, Jul. 2013
3. OpenHEVC decoder: <https://github.com/OpenHEVC/openHEVC>

1. <https://hevc.hhi.fraunhofer.de/svn/svn_SHVCSoftware/>
2. http://gpac.wp.mines-telecom.fr/

# Patent rights declaration(s)

**INSA/IETR Rennes may have current or pending patent rights relating to the technology described in this contribution and, conditioned on reciprocity, is prepared to grant licenses under reasonable and non-discriminatory terms as necessary for implementation of the resulting ITU-T Recommendation | ISO/IEC International Standard (per box 2 of the ITU-T/ITU-R/ISO/IEC patent statement and licensing declaration form).**