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◁JCTVC-L0096▷ Hardware Implementation of a HEVC Decoder

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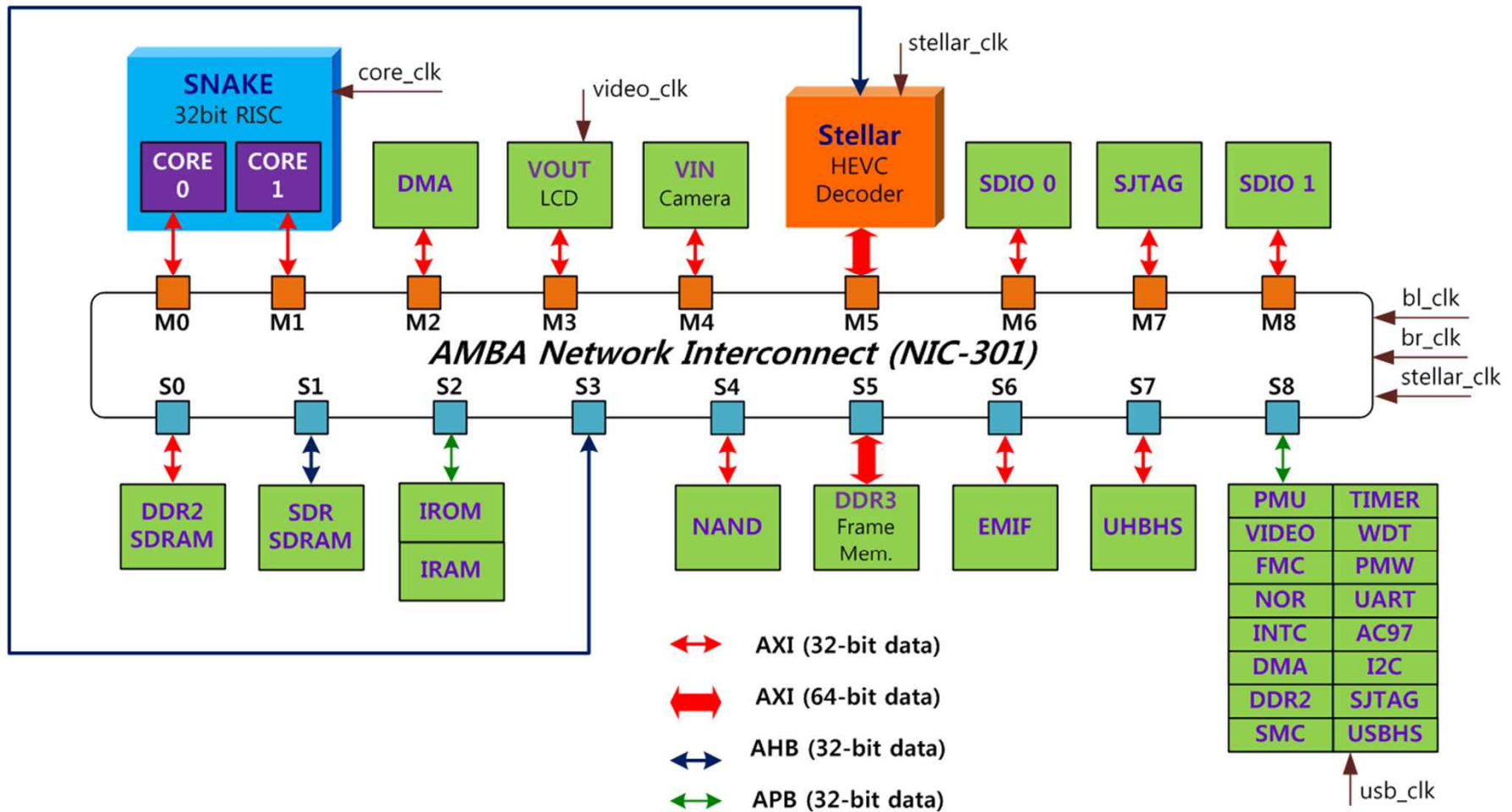


Summary

❑ Implementation of a HEVC hardware decoder

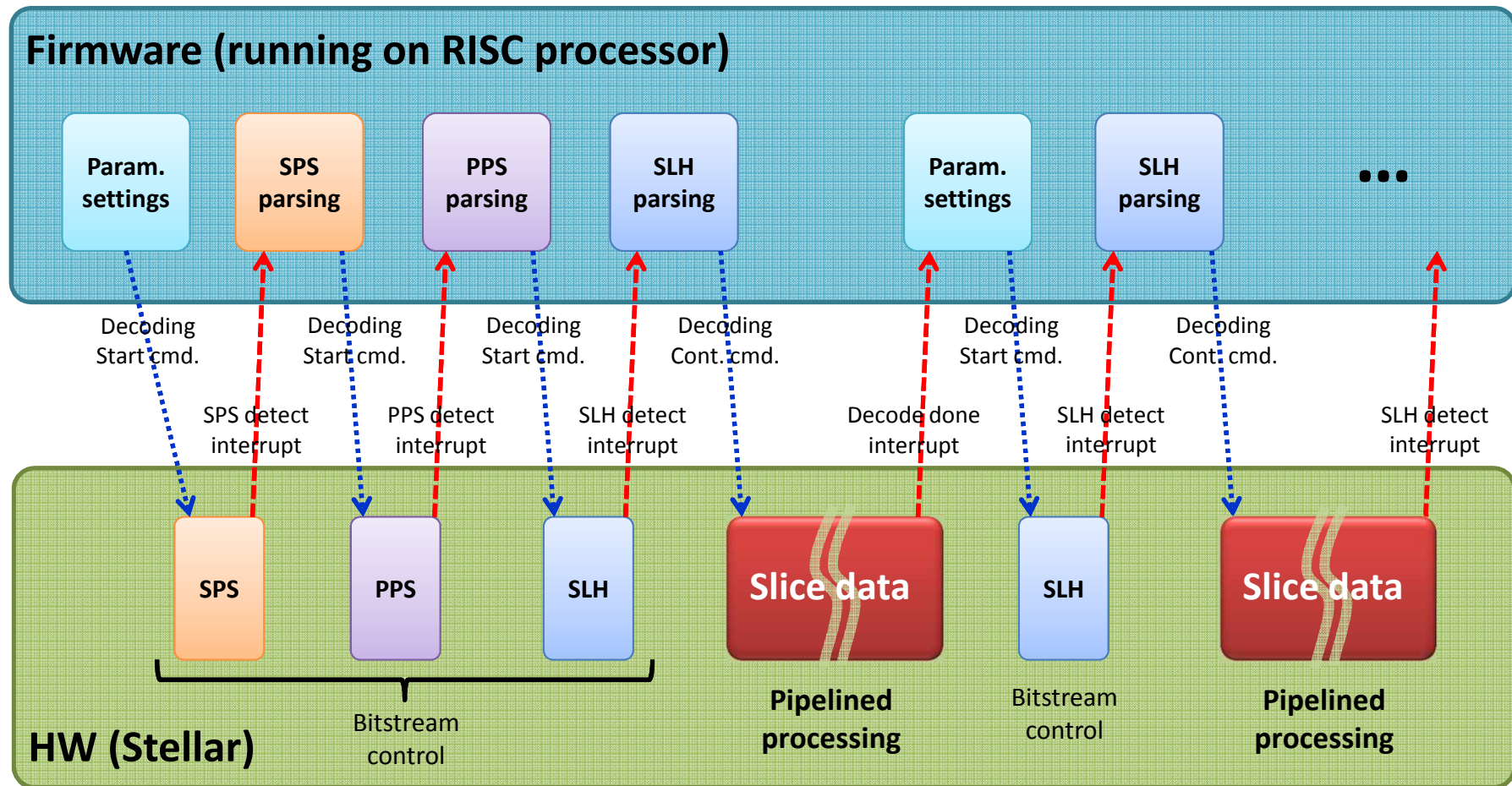
- ❖ Implementation method: Verilog HDL, fully synthesizable
- ❖ Reference HM version: 6.0
- ❖ Target profile / level: HEVC Main profile / 4.3
- ❖ Implementation scheme: dedicated HW cooperating with a RISC processor
 - HW pipeline: CTU based
 - Cache for MC: implemented
- ❖ Bus interface: a 64-bit AMBA AXI master, a 32-bit AMBA AHB slave
- ❖ Performance
 - 1080p@60fps running at 266MHz
 - 720p@30fps running at 58MHz
 - 480p@30fps running at 20MHz
- ❖ HW size (65nm technology)
 - Logic: 1.76 Mgate
 - SRAM: 178KB

System Overview

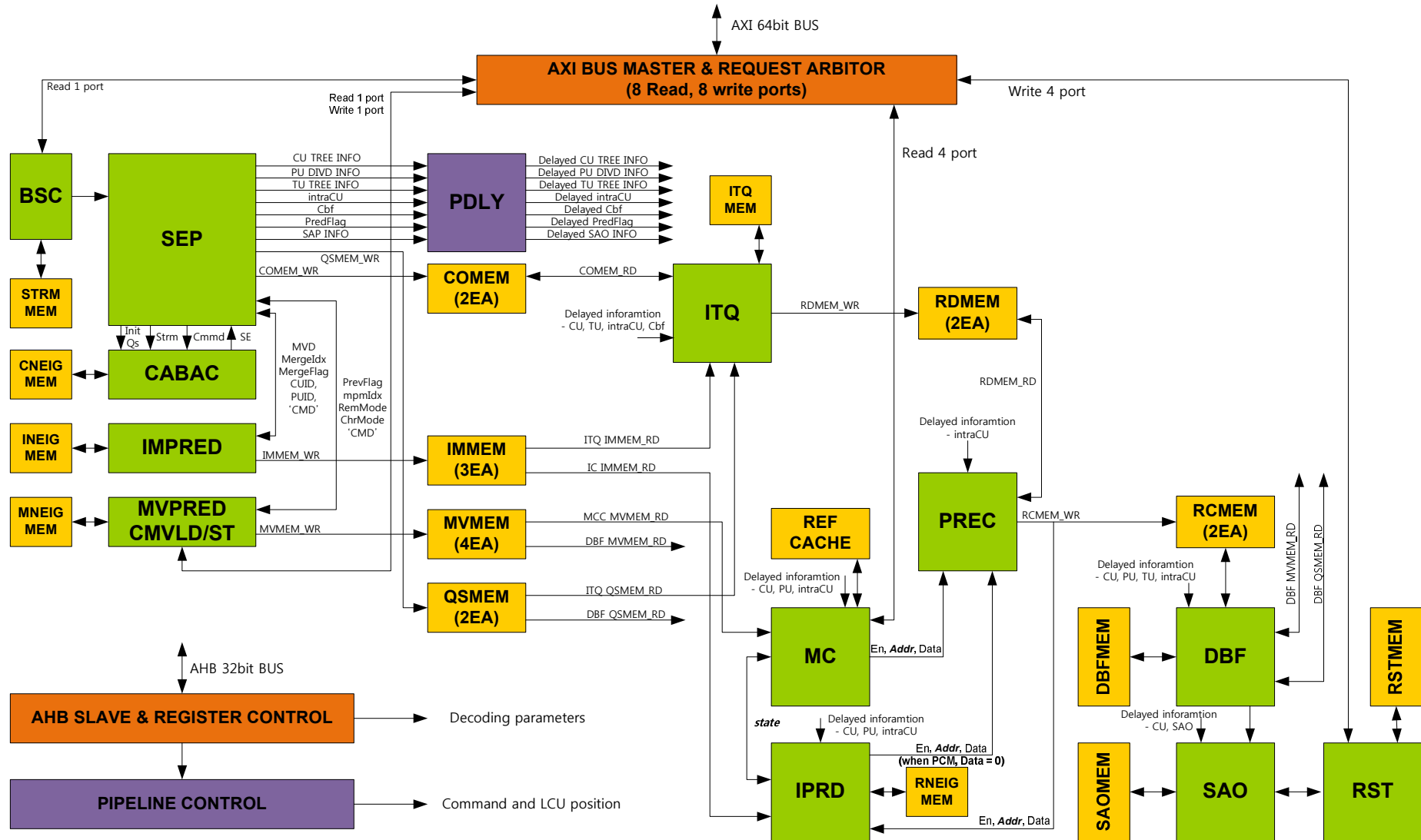


Decoding Process

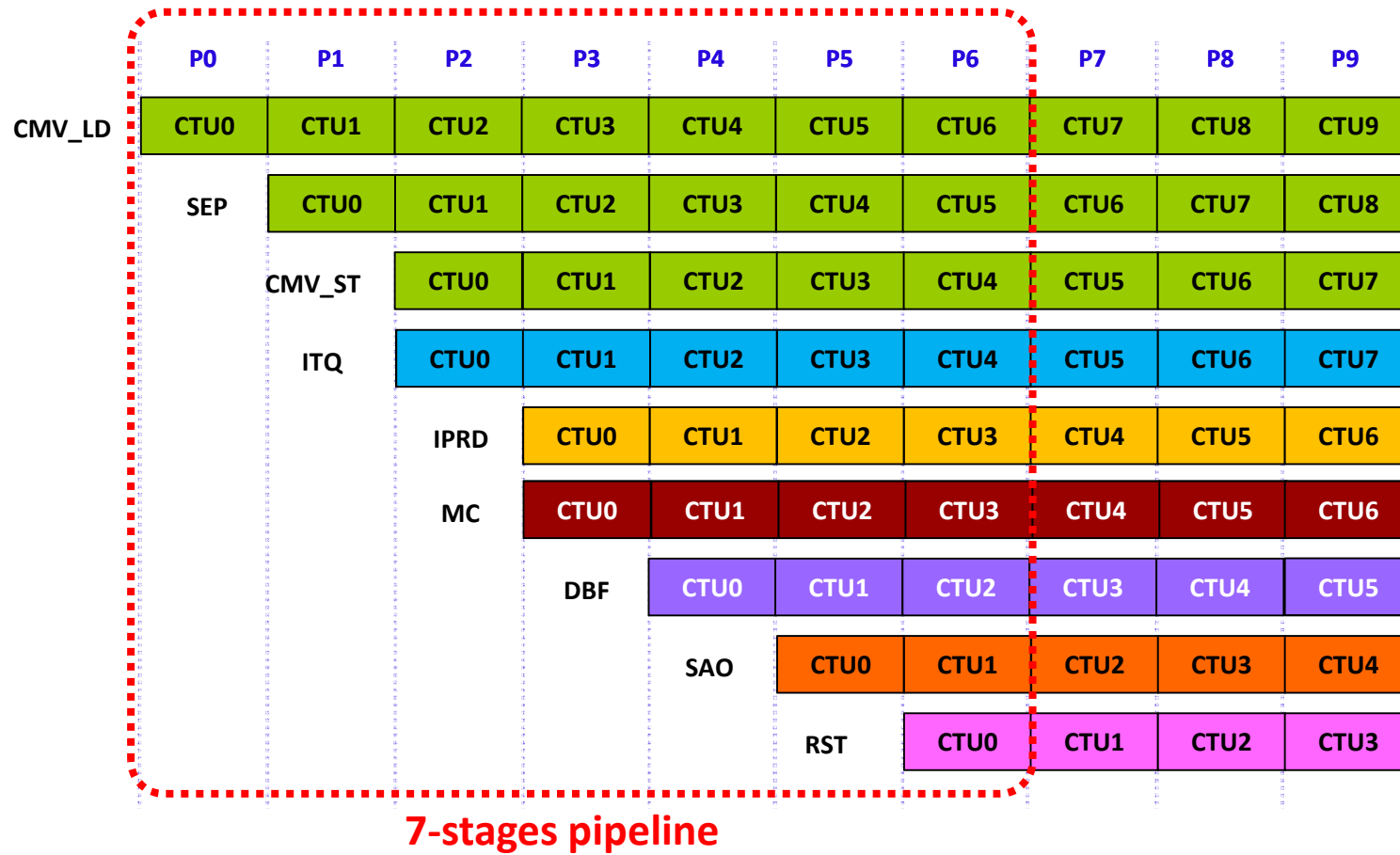
❑ HW/SW co-operations (simplified)



Decoder HW Structure



Pipeline Structure



- CMV_LD : Co-located Motion Vector Load
- SEP : Syntax Element Parsing
- CMV_ST : Co-located Motion Vector Store
- ITQ : Inverse Transform & Quantization
- IPRD : Intra Prediction
- DBF : Deblocking Filter
- SAO : Sample Adaptive Offset
- RST : Recon. Store

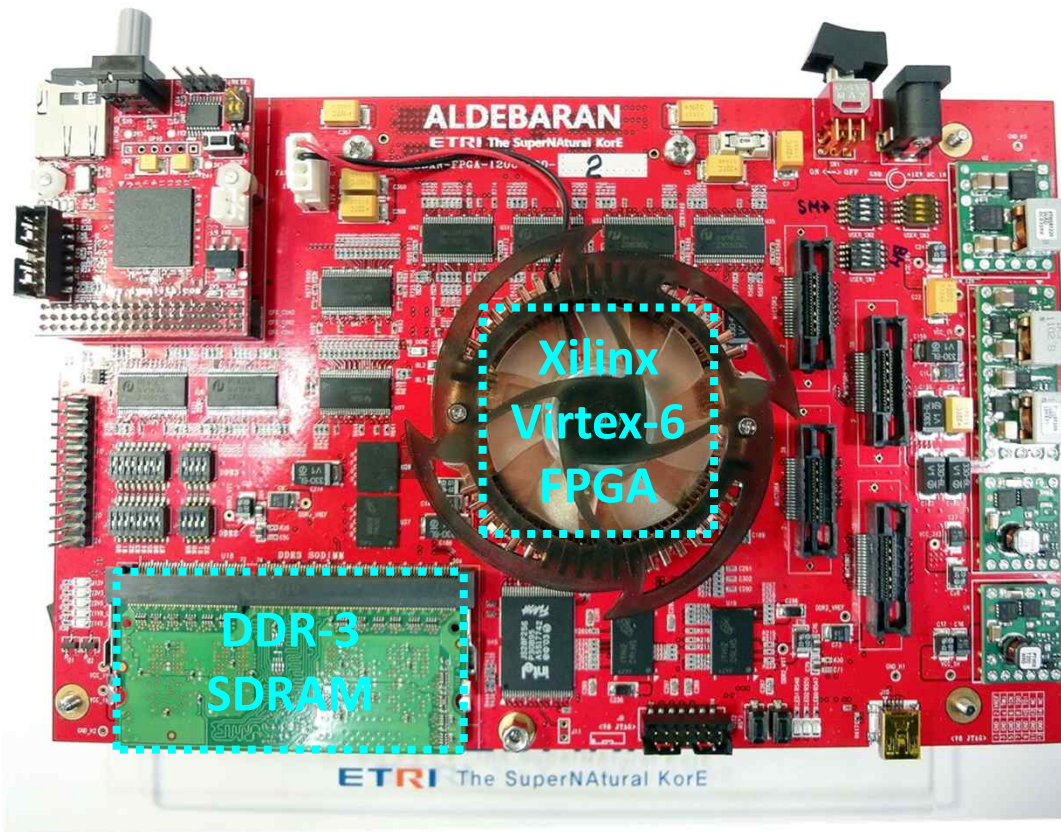
Synthesis Results

Module name	Gate count (K gates)	Frequency (MHz)	SRAM (Kbytes)
SEP (w/ CABAC)	138	>266	1.9
ITQ	779	>266	2
IPRD	270	>266	4.2
MC (w/ Cache)	440	>266	50
DBF	84	>266	16.5
SAO	32	>266	10.3
RST	10	>266	15
Etc.	10	>266	78
Total	1,763	>266	177.9

※ 65nm GP technology is used for synthesis.

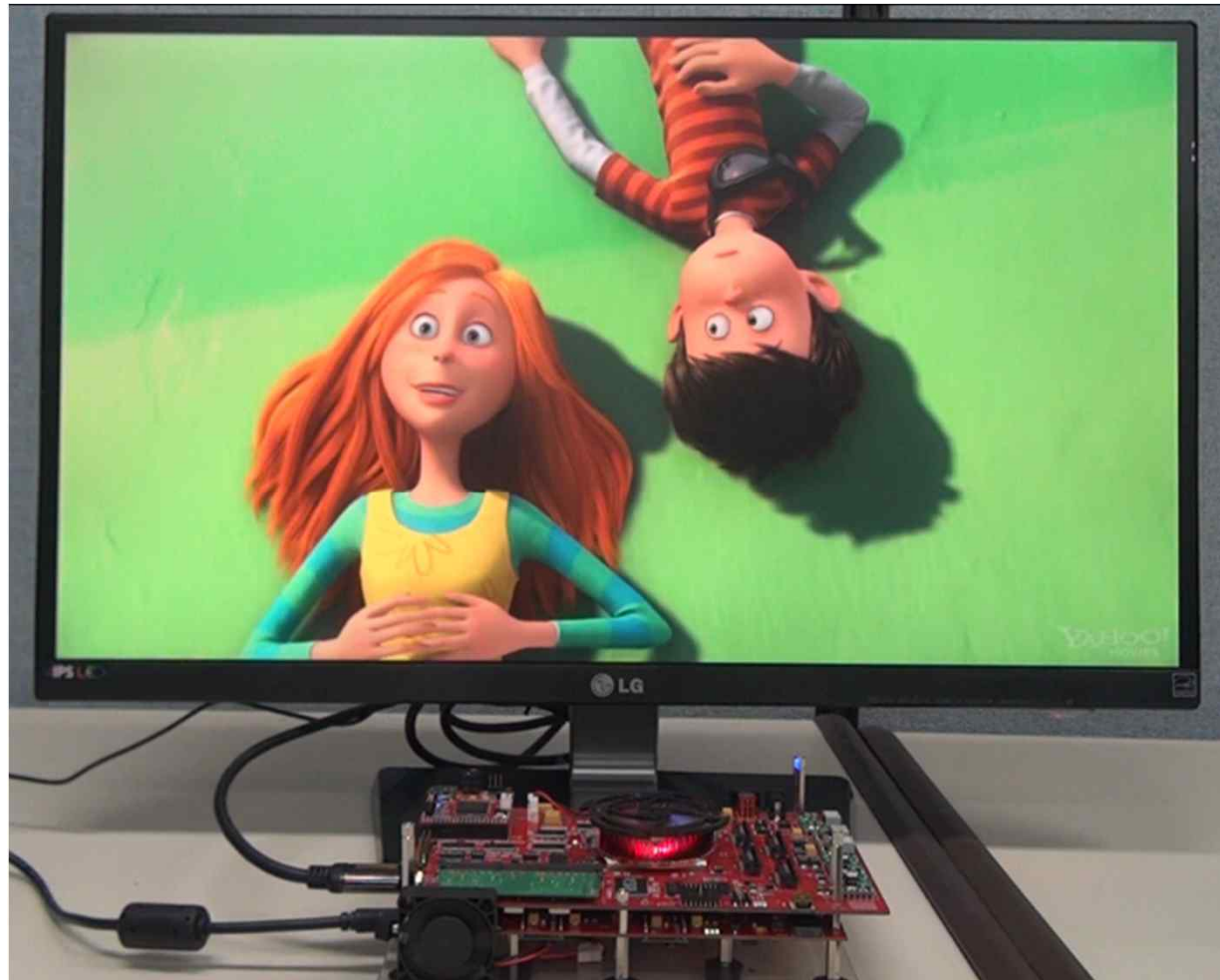
FPGA Prototyping Board

❑ Board snapshot



Feature	Description
FPGA	Xilinx Virtex-6 (XC6VLX760)
Frame Mem.	DDR3 SDRAM (64-bit, SODIMM, 1GB)
Program Mem.	SDR / DDR2 SDRAM (32-bit, 128MB)
Video Output	HDMI
Other I/Os	Full-HD camera, NAND flash, SD, USB, Ethernet, AC97, UART / JTAG, and etc.

Demonstration



Enjoy it in the lounge at coffee break !!



Thank You Very Much !

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