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| --- | --- | --- | --- |
| *Title:* | **AHG7: Disallow bi-predictive mode for 8x4 and 4x8 inter PUs** | | |
| *Status:* | Input Document to JCT-VC | | |
| *Purpose:* | Proposal | | |
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# Abstract

In the current HM7.0 design an encoder is allowed to send bi-predictive motion vectors for inter PUs of 8x4 and 4x8 and a decoder discards list 1 motion vectors for those PUs in order to reduce the worst case memory bandwidth requirements of motion compensation. Such a design may cause design confusion on the encoder side and complicate the decoder design validation unnecessarily. This contribution advocates to prohibit bi-predictive motion vectors for inter 8x4 and 4x8 PUs by modifying the CABAC binarization of inter\_pred\_idc. In the proposed algorithm, the CABAC binarization of inter\_pred\_idc for inter 8x4 and 4x8 PUs is modified to (FL, cMax = 1), i.e. “1” for Pred\_L1 and “0” for Pred\_L0, and for inter PUs of size 8x8 and above the same CABAC binarization process defined in HM7.0 is used, i.e. “1” for Pred\_BI, “01” for Pred\_L1 and “00” for Pred\_L0. Compared to HM7.0, the proposed algorithms leads to an average gain of 0.0/0.0/0.1/0.1 (% in RA-Main/RA-HE10/LB-Main/LB-HE10). Prohibiting bi-pred mode for 8x4 and 4x8 inter-PUs at syntax level is helpful for avoiding potential confusions from both encoder and decoder side.

# Introduction

In the current HM7.0 design an encoder is allowed to send bi-predictive motion vectors for inter PUs of 8x4 and 4x8 and a decoder discards list 1 motion vectors for those PUs in order to reduce the worst case memory bandwidth requirements of motion compensation. Such a design may cause design confusion on the encoder side and unnecessarily complicate the decoder design validation as bi-predictive mode is still a valid mode for 8x4 and 4x8 inter PUs. Confusions may include how bi-predictive motion vectors of 8x4 and 4x8 inter PUs are handled in merging and AMVP candidate list derivation process, whether AMVP candidate list for list 1 still needs to be derived for bi-pred 8x4 and 4x8 inter PUs though list 1 motion vectors are discarded during the motion compensation process.

This contribution advocates prohibiting bi-pred mode for 8x4 and 4x8 inter PUs. The approach to modify the CABAC binarization table of inter\_pred\_idc for 8x4 and 4x8 inter PUs. In the proposed algorithm, the CABAC binarization table of inter\_pred\_idc for 8x4 and 4x8 inter PUs is changed to FL, cMax =1 as shown in Table 1, the CABAC binarization table of inter\_pred\_idc for inter PUs of size 8x8 and above remains unchanged as shown in Table 2.

|  |  |  |  |
| --- | --- | --- | --- |
| **Slice\_type** | **inter\_pred\_idc** | **Name of inter\_pred\_idc** | **bin string** |
| P | inferred | Pred\_L0 | - |
| B | 0 | Pred\_L0 | 0 |
| 1 | Pred\_L1 | 1 |
| 2 | Pred\_BI | - |

**Table 1. CABAC binarization table for inter\_pred\_idc of 8x4 and 4x8 inter PUs (FL, cMAX = 1)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Slice\_type** | **inter\_pred\_idc** | **Name of inter\_pred\_idc** | **bin string** |
| P | inferred | Pred\_L0 | - |
| B | 0 | Pred\_L0 | 00 |
| 1 | Pred\_L1 | 01 |
| 2 | Pred\_BI | 1 |

**Table 2. CABAC binarization table for inter\_pred\_idc of inter PUs of size 8x8 and above (same as HM7.0)**

The proposed method introduces the least amount of changes relative to the current design. In HM7.0 an 8x4 or 4x8 inter PU can have list0 uni-prediction, list 1 uni-prediction or bi-predication mode. With the proposed change, the bi-prediction mode is prohibited for 8x4 or 4x8 inter PUs at syntax level.

# Test Settings and Conditions

The simulations of this document have used HM7.0 software, the simulation platform is LSF equipped with Intel(R) Xeon(R) CPU X5570 64 bits Linux machines of different frequencies, the common test conditions and reference configurations specified in [1] are followed.

# Experimental results

Table 3 summarizes the experimental results of proposed algorithm. By fixing the inter\_pred\_idc coding for 8x4 and 4x8 inter PUs, an average gain of 0.0/0.0/0.1/0.1 (% in RA-Main/RA-HE10/LB-Main/LB-HE10) is observed.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Random Access Main** | | | **Random Access HE10** | | |
|  | Y | U | V | Y | U | V |
| Class A | 0.0% | -0.1% | -0.1% | 0.0% | 0.0% | 0.1% |
| Class B | 0.0% | 0.0% | 0.0% | 0.0% | 0.0% | 0.0% |
| Class C | -0.1% | 0.0% | 0.0% | -0.1% | 0.0% | -0.1% |
| Class D | -0.1% | 0.1% | -0.2% | -0.1% | 0.0% | -0.1% |
| Class E |  |  |  |  |  |  |
| **Overall** | 0.0% | 0.0% | -0.1% | 0.0% | 0.0% | -0.1% |
|  | 0.0% | 0.0% | -0.1% | 0.0% | 0.0% | -0.1% |
| Class F | 0.0% | 0.0% | 0.1% | 0.0% | 0.1% | 0.0% |
| Enc Time[%] | 98% | | | 98% | | |
| Dec Time[%] | 97% | | | 96% | | |
|  |  | | |  | | |
|  | **Low delay B Main** | | | **Low delay B HE10** | | |
|  | Y | U | V | Y | U | V |
| Class A |  | | |  | | |
| Class B | 0.0% | 0.1% | 0.2% | 0.0% | 0.1% | 0.2% |
| Class C | -0.1% | 0.1% | -0.1% | -0.1% | -0.2% | 0.2% |
| Class D | -0.1% | -0.2% | 0.3% | -0.2% | -0.2% | -0.2% |
| Class E | 0.0% | 0.2% | -0.1% | 0.1% | 0.0% | 0.4% |
| **Overall** | -0.1% | 0.0% | 0.1% | -0.1% | -0.1% | 0.1% |
|  | -0.1% | 0.0% | 0.1% | -0.1% | 0.0% | 0.2% |
| Class F | -0.1% | 0.6% | -0.1% | 0.0% | -0.1% | 0.9% |
| Enc Time[%] | 102% | | | 99% | | |
| Dec Time[%] | 101% | | | 98% | | |

**Table 3. Experimental results of proposed algorithm**

# Conclusions

# The proposed algorithm prohibits bi-predictive mode for 8x4 and 4x8 inter PUs and avoids potential confusions from both encoder and decoder side. It is recommended to adopt the proposed change to clean up the current design.

# References

[1] F. Bossen, “Common test conditions and software reference configurations,” JCT-VC Document, JCTVC-I1100, 9th Meeting: Geneva, Switzerland, 27 April – 07 May, 2012

[2] [B. Bross](mailto:benjamin.bross@hhi.fraunhofer.de), [W.-J. Han](mailto:wjhan.han@samsung.com), [J.-R. Ohm](mailto:ohm@ient.rwth-aachen.de), [G. J. Sullivan](mailto:garysull@microsoft.com), [T. Wiegand](mailto:thomas.wiegand@hhi.fraunhofer.de) “High Efficiency Video Coding (HEVC) text specification draft 7,” JCT-VC Document, JCTVC-I1003, 9th Meeting: Geneva, Switzerland, 27 April – 07 May, 2012.

[3] S. Fukushima, M. Ueda and H. Takehara, “AHG7: Bi-pred restriction for small PUs,” JCT-VC Document, JCTVC-I0297, 9th Meeting: Geneva, Switzerland, 27 April – 07 May, 2012

# Patent rights declaration(s)

**Texas Instruments, Inc. may have IPR relating to the technology described in this contribution and, conditioned on reciprocity, is prepared to grant licenses under reasonable and non-discriminatory terms as necessary for implementation of the resulting ITU-T Recommendation |ISO/IEC International Standard (per box 2 of the ITU-T/ITU-R/ISO/IEC patent statement and licensing declaration form).**

# CD text

In Table 9‑39 – Assignment of ctxIdxInc to binIdx for all ctxIdxTable and ctxIdxOffset values

| **Syntax element** | **ctxIdxTable,  ctxIdxOffset** | | **binIdx** | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **0** | **1** | **2** | **3** | **>=4** |
| inter\_pred\_idc |  | 0 | If (nPSW + nPSH != 12) ctDepth  Otherwise  4 | If (nPSW + nPSH != 12)  4  Otherwise  na | na | na | na |

#### 9.2.2.x Binarization process for inter\_pred\_idc

Input to this process is a request for a binarization for the syntax element inter\_pred\_idc, slice\_type and variables specifying the width and the height of the prediction unit, nPSW and nPSH.

Output of this process is the binarization of the syntax element.

The binarization for inter\_pred\_idc is given by Table 9-xx depending on inter\_pred\_idc, slice\_type and prediction unit size nPSW and nPSH.

Table 9‑xx – Binarization for inter\_pred\_idc

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **slice\_type** | **inter\_pred\_idc** | **Name of inter\_pred\_idc** | **Bin String** | | |
| nPSW + nPSH != 12 | nPSW + nPSH == 12 | |
| P | inferred | Pred\_L0 | - | - | |
| B | 0 | Pred\_L0 | 00 | | 0 |
| 1 | Pred\_L1 | 01 | | 1 |
|  | 2 | Pred\_BI | 1 | | - |