



AHG6: Comparison between ALF and bi-prediction MC in low-delay conditions

Ching-Yeh Chen, Chia-Yang Tsai, Yung-Chang Chang, Chia-Yun Cheng, Fu Chun Yeh,
Hao-Wei Li, Tzu-Der Chuang, Yu-Wen Huang, Shawmin Lei (MediaTek)



Presented by Yu-Wen Huang
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Overall Summary

- Comparison ALF and Bi-Prediction MC in low-delay conditions
 - 15 full HD sequences: 5 from CTC class B and 10 from KTA 1080p

Anchor: Main-LP, ALF-off	ALF (Main-LP, ALF-on)	Bi-Prediction MC (Main-LB, ALF-off)
BD-rate	-8.3%	-10.5%
HM Encoding Time	100%	140%
HM Decoding Time	116%	109%
MC Bandwidth	99%	161%

- Off-chip DRAM power is 251X of on-chip SRAM
- Off-chip DRAM latency is 26X of on-chip SRAM
- For real-time low-delay encoding-decoding applications (e.g. video phones and video conferencing) with full HD resolution, ALF could be a better trade-off than bi-prediction MC.

Power Consumption

- In 40nm silicon technology, the power consumption of data access in different memory types for accessing 64 bits.

Memory Type	Power (pW)	Latency
DRAM	1399.60	26T
SRAM512x64SP (Read/Write)	5.57	1T
SRAM512x64SP (Write)	8.18	1T
Register (Read)	0.37	< 1T
Register (Write)	0.94	< 1T

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Thank you



BD-Rates & Run Times

- 15 full HD sequences
 - 5 sequences from Class B of CTC
 - 10 sequences from KTA
- Anchor: Main-LP without ALF
 - ALF preserves 79% of the coding gain achieved by Main-LB without ALF.

	Main-LP with ALF			Main-LB without ALF		
BD-Rate	Y	U	V	Y	U	V
CTC FHD	-6.1%	-5.0%	-4.1%	-11.4%	-10.3%	-10.0%
KTA FHD	-9.5%	-5.3%	-5.3%	-10.0%	-9.3%	-8.6%
Average	-8.3%	-5.2%	-4.9%	-10.5%	-9.6%	-9.1%
Enc. Time	100%			140%		
Dec. Time	116%			109%		

Power Consumption

- A H.264/AVC decoder takes 42.3mW when decoding a full HD 60fps bitstream.
 - Normalized to 40nm silicon technology
- DRAM power consumption
 - Data access includes MC bandwidth and the bandwidth of decoded pictures
 - MC bandwidth is gathered from the bitstreams in previous experiments and normalized to the specification of full HD 60fps.

	Main-LP, ALF-Off	Main-LP, ALF-On	Main-LB, ALF-Off
DRAM Access (MB/s)	348.6 (Read) + 186.6 (Write)	345.3 (Read) + 186.6 (Write)	551.5 (Read) + 186.6 (Write)
Power (mW)	93.6	93.1	129.1

- Main-LB without ALF needs more 35.5mW in power consumption, which is roughly equal to 20%-30% power increase of the entire decoding system (Decoder+DRAM)