



# **AHG4: Profile Requirements For Facilitation Of Parallel Tile Decoding**

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- Existing Main Profile restrictions on tiles are not sufficient for parallel decoding by systems where feedback/capability negotiation is available
  - E.g. broadcast
- Height and width of tiles should be tightly specified to make it practical to implement level conforming parallel decoders
- Proposal: modify profile specifications to restrict width and height of tiles

- Option 1
  - Specify large tile sizes, mapping tile sizes to levels
  - Using fewer tile sizes is compression efficient, but has poor flexibility and load balancing
  - Restricts number of cores that can be used by the encoder and decoder
- Option 2 (recommended)
  - Specify smaller, fixed tile sizes
  - Better load balancing
  - Makes parallel decoder implementation easier, as there is more flexibility to choose different numbers of cores at the encoder and decoder
  - This option achieves a similar level of flexibility to WPP
  - Less compression efficient

# Proposed Limitations

- $\text{uniform\_spacing\_flag} = 1$
- $\text{ColumnWidthInLumaSamples}[i]$  shall be greater than or equal to 384 for any  $i$  in the range of 0 to  $\text{num\_tile\_columns\_minus1}$ , inclusive
- $\text{num\_tile\_columns\_minus1} = \text{Floor}(\text{PicWidthInCtbs} / (6 * 2^{6 - \text{Log2CtbSize}})) - 1$ 
  - This restricts the number of tile columns irrespective of CTB size
  - $64 * 6 = 384$
- $(\text{num\_tile\_columns\_minus1} + 1) * (\text{num\_tile\_rows\_minus1} + 1) < \text{Ceil}(\text{pic\_height\_in\_luma\_samples} / 64)$
- $\text{ColumnHeightInLumaSamples}[i]$  shall be greater than or equal to 256 for any  $i$  in the range of 0 to  $\text{num\_tile\_rows\_minus1}$ , inclusive

# Example Tile Specifications

- The proposed profile settings should provide the following example tile rows and columns

Class	LumaWidth	LumaHeight	num_tile_columns	num_tile_rows
A	2560	1600	6	5
B	1920	1080	5	4
C	832	480	2	2
E	1280	720	3	3

- Tile height and width should be tightly constrained to allow parallel decoder implementation
- Using smaller tiles provides better functionality at the cost of some compression efficiency
- Larger tiles are not effective for load balancing, and restrict parallelism to levels below those currently exploited
- Recommend adopting smaller tile specifications, where size of a tile is relatively consistent
- Proposed restrictions are in effect set according to picture resolution, rather than levels, which are more loosely linked with resolution
  - Level settings may allow implementers to choose unexpected combinations of tiles and resolution, by choosing a higher level