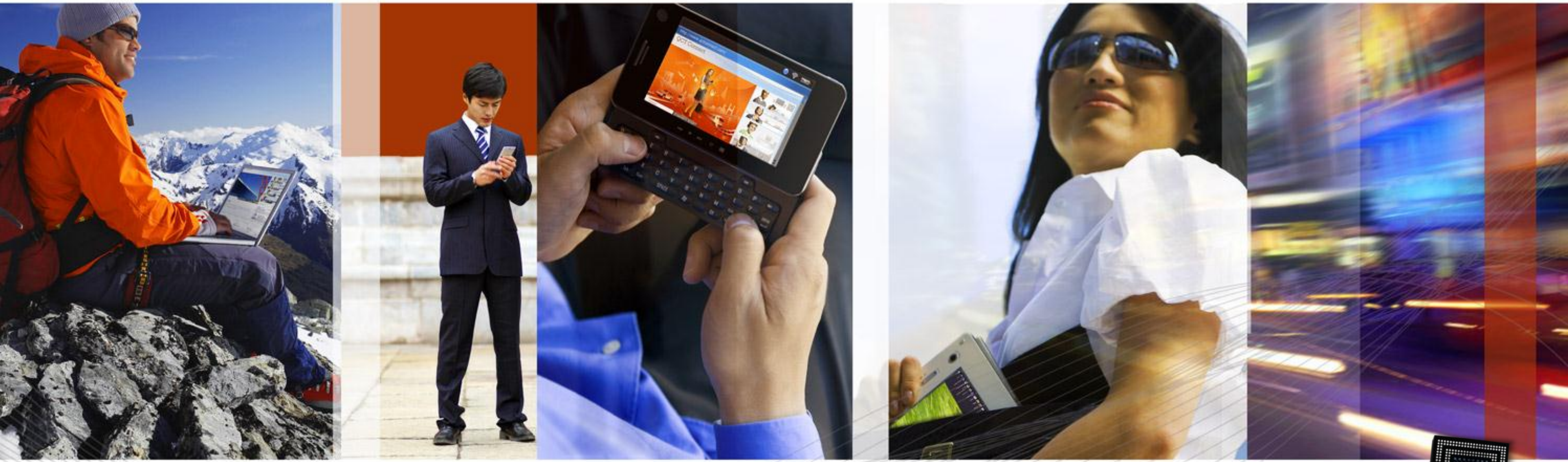


QUALCOMM CDMA Technologies

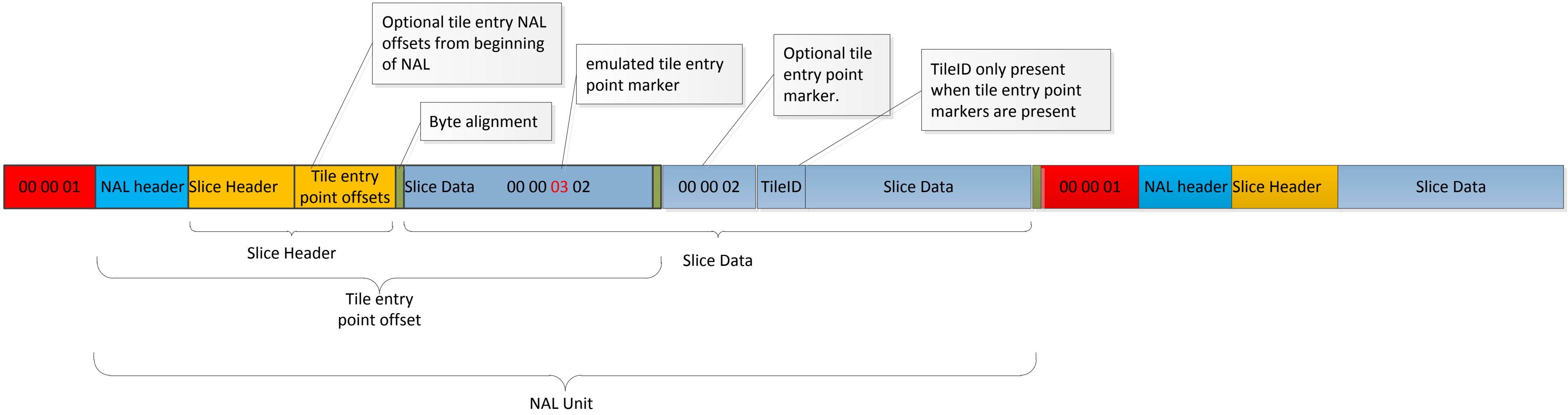
REDEFINING MOBILITY

JCTVC-I0357
Tile entry point signalling

M. Coban, Y.-K. Wang, M. Karczewicz

Current tile entry point signalling scheme

- Entry point NAL unit offsets relative to the previous entry point starting from the beginning of the NAL unit.
- Tile start code markers (entry_point_marker_two_3bytes = 0x000002) at byte aligned positions before the start of each tile.
- Allows existence of both types of tile entry point signalling concurrently or separately.



Issues with current scheme

- Tile entry offsets are signaled in the slice header that is in the RBSP structure; however the offsets signaled in the slice header are byte offsets in the NAL unit structure. Handling of emulation prevention bytes becomes tricky.
- It is not mandated that each tile entry will have a tile entry point marker. Parser cannot differentiate between tile entry marker bits and emulated tile entry marker bits.
- When tile entry markers are not present, then the TileID field is not present. In this case even if the decoder knows the bitstream entry point to the start of a tile, it doesn’t know the physical address of the tile within a picture.

Proposed changes

- Tile entry points signalled in the slice header should be relative RBSP offsets from the previous tile entry point, starting from the end of the slice header, i.e. beginning of the slice data.
- If entry points are signalled then TileID should be present for every tile with entry point, its value being the tile number in tile raster order of the picture, starting from 0, for enabling parallel decoding.
- If tile entry markers (0x000002) are used, then they should be present for every tile.
- Presence of entry offsets in the slice header or tile start code markers are signaled in SPS.

WD changes

seq_parameter_set_rbsp( ) {	Descriptor
profile_idc	u(8)
……..	
tiles_or_entropy_coding_sync_idc	u(2)
if(tiles_or_entropy_coding_sync_idc = = 1) {	
num_tile_columns_minus1	ue(v)
num_tile_rows_minus1	ue(v)
uniform_spacing_flag	u(1)
if(!uniform_spacing_flag) {	
for(i = 0; i < num_tile_columns_minus1; i++)	
column_width[i]	ue(v)
for(i = 0; i < num_tile_rows_minus1; i++)	
row_height[i]	ue(v)
}	
loop_filter_across_tiles_enabled_flag	u(1)
tile_entry_point_idc	u(2)
}	
vui_parameters_present_flag	u(1)

slice_header( ) {	**Descriptor**
first_slice_in_pic_flag	u(1)
………	
if(tiles_or_entropy_coding_sync_idc > 0) {	

if((tile_entry_point_idc & 0x02) ||
(tiles_or_entropy_coding_sync_idc = = 2)){	

num_entry_point_offsets	ue(v)
if(num_entry_point_offsets > 0) {	
offset_len_minus1	ue(v)
for(i = 0; i < num_entry_point_offsets; i++)	
entry_point_offset[i]	u(v)
}	
}	
}	
}	

WD changes

slice_data( ) {	**Descriptor**
CtbAddrRS = SliceCtbAddrRS	
…….	
if(moreDataFlag && ((tiles_or_entropy_coding_sync_idc = = 1 && TileId[CtbAddrTS] != TileId[CtbAddrTS − 1]) | | (tiles_or_entropy_coding_sync_idc = = 2 && num_substream_minus1 > 0 && CtbAddrTS / PicWidthInCtbs <= num_substream_minus1 && CtbAddrTS % PicWidthInCtbs = = 0))) {	
rbsp_trailing_bits( )	
if(tile_entry_point_idc & 0x01)	
entry_point_marker_two_3bytes	f(24)
if(tiles_or_entropy_coding_sync_idc = = 1 && tile_entry_point_idc)	
tile_idx_minus_1	u(v)
}	
} while(moreDataFlag)	
}	

7.3.2.1 Sequence parameter set semantics

tile_entry_point_idc indicates the presence of tile entry points signaling fields in the slice header (when the first bit is equal to 1) and the entry_point_marker_two_3bytes at the beginning of each tile (when the second bit is equal to 1). When not present, the value of tile_entry_point_idc is inferred to 0 (both bits are equal to 0).