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| **Joint Collaborative Team on Video Coding (JCT-VC)**  **of ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11**  8th Meeting: San Jose, CA, USA, 1-10 February, 2012 | Document: JCTVC-H0010  M23286 |

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| *Title:* | JCT-VC AHG report: Parallel merge/skip (AHG 10) | | |
| *Status:* | [Input Document] | | |
| *Purpose:* | Report | | |
| *Author(s) or Contact(s):* | Minhua Zhou (Chair)  Texas Instruments Inc  Hui Yong Kim (Vice-Chair) ETRI (Electronics and Telecommunications Research Institute)  Patrice ONNO (Vice-Chair)  Canon Research Centre France  Xing Wen (Vice-Chair)  The Hong Kong University of Science and Technology | Email: | zhou@ti.com  hykim5@ etri.re.kr  [patrice.onno@crf.canon.fr](mailto:patrice.onno@crf.canon.fr)  [wxxab@ust.hk](mailto:wxxab@ust.hk) |
| *Source:* | Parallel merge/skip AHG | | |

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# Abstract

This document summarizes the AHG activities between 7th Meeting: Geneva, 21-30 November, 2011, and the current 8th Meeting: San Jose, CA, USA, 1-10 February, 2012.

# Mandate

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| **AHG Title and Email Reflector** | **Chairs** | **Mtg** |
| **Parallel merge/skip (AHG10)**  ([jct-vc@lists.rwth-aachen.de](mailto:jct-vc@lists.rwth-aachen.de" \o "mailto:jct-vc@lists.rwth-aachen.de blocked::mailto:jct-vc@lists.rwth-aachen.de))   1. Develop common understanding of underlying motion estimation throughput issues due to sequential merge mode 2. Evaluate parallel merge/skip solutions including configurable and CU-based approaches 3. Work on alternative solutions that would narrow the performance gap between parallel and non-parallel merge 4. Report the results of these studies, discussions and experiments to the JCT-VC 5. Recommend a unified solution if available | M. Zhou (chair), H. Y. Kim, P. Onno, X. Wen (vice chairs) | N |

# Related activities and input contributions

**Related to Mandate 1:**

The AHG had a short meeting in Geneva and active e-mail discussions between the meetings. The general understanding of underlying motion estimation throughput issues is as follows:

1. There is motion estimation throughput issue on the encoder side due to dependency of merge/skip MVP list (MCL) derivation on the regular motion estimation, if an encoder chooses to leverage full quality potential of HEVC merge/skip mode.
2. Excessive amount of MCL derivation required for motion estimation worsens the motion estimation throughput issue.

**Figure 1. Motion estimation throughput comparison between AVC and HEVC at 16x16 block level.**

Motion estimation is bottleneck on the encoder side, the motion estimation throughput is dictated by the regular motion estimation. As shown in Figure 1, in AVC the skip MV derivation and skip search are on 16x16 block level and can be fully parallelized with the regular motion estimation (see AVC ME timing diagram in Figure 1). In HEVC, quality is improved in this particular example because not only 16x16 block level but also sub-16x16 level merge/skip is supported by the standard. However, because of inter-dependency of the MCL derivation, in this case only the MCL derivation and merge motion of the first 8x8 CU (i.e. CU0) and 16x16 CU can run parallel to the regular ME, the MCL derivation and merge motion of other CUs can only run sequentially after the regular ME is done, which costs additional cycles. Therefore, to exploit full quality potential of HEVC, a HEVC encoder needs more time to complete the motion estimation.

Two architectures were proposed to quantify the quality loss of HM5 in parallel motion estimation (PME) environment, namely HM5 PME A and HM5 PME B. Note that in HM5 PME A and B the TMVP reference index is set to 0 for merge/skip list derivation to decouple the CU-level MCL dependency. In the current HM5 the TMVP reference index is NOT set to 0 for MCL derivation.

As shown in Figure 2, in HM5 PME A, an encoder chooses to skip MCL derivation and thus the merge estimation for those PUs/CUs whose MCLs cannot be constructed due to the PME constraints (so-called affected PUs/CUs hereafter), which causes quality loss but meets the throughput requirements.

In HM5 PME B, instead of simply dropping MCL/MME for affected PUs/CUs, an encoder constructs partial MCL for those affected PUs/CUs with available MVPs, and enables MME for the affected PUs/CUs as well with partial MCLs. In this case, no accurate RDO cannot be done for MME of affected PUs/CUs because the partial MCLs are incomplete, which also causes quality loss. In addition, accurate MCL derivation and merge index matching needs to be done for the merge\_idx coding. This requires extra logic and cycles, and needs to done outside the ME engine because of ME cycle constraints.

**Figure 2. Potential motion estimation architectures for HM5 in parallel ME environment.**

|  |  |  |
| --- | --- | --- |
| **ME Engine** | **# of MCLs w/o AMP** | **# of MCLs w/ AMP** |
| 64x64 | 5 | 13 |
| 32x32 | 4 x 5 | 4 x 13 |
| 16x16 | 16 x 5 | 16 x 13 |
| 8x8 | 64 x 5 (no 4x4) | 64 x 5 (no 4x4) |
| Total | 425 | 593 |

**Table 1. Number of MCLs for motion estimation of a 64x64 LCU**

Another issue identified is number of MCLs. Table 1 lists the total number of MCLs needed for the brute force motion estimation of a 64x64 LCU (with and without AMP). This amount of MCL derivation is not practical in actual real-time implementations due to high area cost and memory access congestion. Therefore, this is a need to reduce the number of MCLs, especially for 8x8 CUs.

Furthermore, due to dependency of merge/skip TMVP reference index derivation, the MCL derivation for the second PU of part mode PART\_Nx2N, PART\_nLx2N, PART\_nRx2N is still dependent on the first PU in the current HM5.0 design. Finally, the MCL derivation of second, third and fourth PU in a CU of PART\_NxN is inter-dependent.

Therefore, the general design goals of parallel merge/skip are:

1. Decouple the merge/skip MVP list derivation process and merge motion estimation from the regular motion estimation, so that both threads can run fully parallel
2. Reduce the number of merge/skip MVP list derivation
3. Remove remaining dependency at CU and SCU level
4. Configurable to enable flexible coding efficiency and throughput trade-offs on the encoder side.

**Related to Mandate 2 and 3:**

Contributions of the CU-group level, CU-level and SCU-level parallel merge/skip were submitted. This section explains basic motivation of those proposals and lists the related contributions.

**Figure 3. Architecture comparison between HM5 PME w/ parallel merge/skip and HM5 PME B**

The CU-group level parallel merge/skip is motivated by making implementation of HM5 PME B architecture simpler and more efficient. The basic idea is to enable full parallel MCL derivation for all PUs/CUs inside a parallel ME region. For the affected PUs/CUs in which spatial neighbouring MVPs for MCL are partially unavailable due to the PME constraints, only those available MVPs are used for the MCL derivation, the unavailable ones can be either excluded or replaced with ones outside the parallel ME region. The remaining MCL derivation process is exactly the same as the HM5.0, i.e. additional MVPs such as combined, non-scaled and zero MVPs are added to the list to form a complete MCL for affected Pus/Cus. As shown in Figure 3, the parallel merge/skip fully decouples MCL derivation and merge ME from the regular ME, and enables accurate RDO for all the PUs/CUs of a parallel ME region without needs of deriving MCLs outside the ME engine for merge\_idx coding.

The following contributions are configurable and enable CU-group level of decoupling of merge/skip MVP list derivation and merge estimation from the regular motion estimation.

|  |  |  |
| --- | --- | --- |
| Document | Title | Proponents |
| [JCTVC-H0082](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4383) | AHG10: Configurable and CU-group level parallel merge/skip | [M. Zhou (TI)](mailto:zhou@ti.com) |
| [JCTVC-H0090](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4391) | AHG10: Unified design on parallel merge/skip | [Y. Jeon](mailto:yongjoon.jeon@lge.com), [B. Jeon (LG)](mailto:bm.jeon@lge.com), [M. Zhou (TI)](mailto:zhou@ti.com), [X. Wen](mailto:wxxab@ust.hk), [O. C. Au (HKUST)](mailto:eeau@ust.hk), [H. Y. Kim (ETRI)](mailto:hykim5@etri.re.kr), [K. Y. Kim (KHU)](mailto:kimky@khu.ac.kr) |
| [JCTVC-H0](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4391)247 | AHG10: Unified design on parallel merge/skip with reduced candidates | [H. Y. Kim (ETRI)](mailto:hykim5@etri.re.kr), [K. Y. Kim (KHU)](mailto:kimky@khu.ac.kr), [Y. Jeon](mailto:yongjoon.jeon@lge.com), [B. Jeon (LG)](mailto:bm.jeon@lge.com), [M. Zhou (TI)](mailto:zhou@ti.com), [X. Wen](mailto:wxxab@ust.hk), [O. C. Au (HKUST)](mailto:eeau@ust.hk) |
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| [JCTVC-H0220](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4523) | AHG10: Cross-check report of TI's configurable and CU-group level parallel merge/skip (JCTVC-H0082) by Panasonic | [T. Sugio](mailto:sugio.toshiyasu@jp.panasonic.com), T. Nishi (Panasonic) |
| [JCTVC-H0369](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4672) | AHG10: Cross-check of configurable and CU-group level parallel merge/skip (JCTVC-H0082) | J. Xu (Microsoft) |
| [JCTVC-H0580](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4891) | AHG10: Crosscheck of TI's Configurable and CU-group level parallel merge/skip (JCTVC-H0082 combination case) | T. Ikai (Sharp) |
| JCTVC-H0681 | AHG10: Cross-check of TI's configurable and CU-group level parallel merge/skip (JCTVC-H0082) by Sony | [J. Xu](mailto:jun.xu@am.sony.com), [A. Tabatabai (Sony)](mailto:ali.tabatabai@am.sony.com) |
| [JCTVC-H0591](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4905) | AhG10: Cross-verification of JCTVC-H0090 on unified design on parallel merge/skip | V. Seregin, X. Wang, J.Chen (Qualcomm) |
| [JCTVC-H0572](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4882) | AHG10: Crosscheck |  |
| [JCTVC-H0](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4391)635 | Cross verification of AHG10: Unified design on parallel merge/skip with reduced candidates | C. Kim (Samsung) |

The CU-level parallel merge/skip is motivated by the fact that in HM5.0 the MCL derivation of the second PU of part mode PART\_Nx2N, PART\_nLx2N, PART\_nRx2N is still dependent on the first PU (see Figure 4). To break this dependency, it is proposed to modify the TMVP reference index derivation process. This category of proposals makes MCL derivation fully independent for PUs of all CUs, except for SCUs of PART\_NxN mode.



**Figure 4. Examples of a neighboring PU of the same CU is referred in the TMVP reference index derivation [from JCTVC-H0092].**

The following contributions enable CU level of parallel merge/skip.

|  |  |  |
| --- | --- | --- |
| Document | Title | Proponents |
| [JCTVC-H0092](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4393) | Non-CE9: Removing PU dependency in TMVP reference index derivation | [Y. Jeon](mailto:yongjoon.jeon@lge.com), [B. Jeon (LG)](mailto:bm.jeon@lge.com), [V. Seregin](mailto:vseregin@qualcomm.com), [X Wang](mailto:xianglin@qualcomm.com), [J. Chen](mailto:cjianle@qualcomm.com), [M. Karczewicz (Qualcomm)](mailto:martak@qualcomm.com) |
| [JCTVC-H0214](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4517) | Non-CE9: Modification of derivation process for the reference index for temporal merging candidate | [T. Sugio](mailto:sugio.toshiyasu@jp.panasonic.com), T. Nishi (Panasonic |
| [JCTVC-H0199](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4501) | Non-CE9: Derivation process of reference indices for temporal merging candidates | [H. Nakamura](mailto:nakamura.hiroya@jvckenwood.com), S. Fukushima (JVC Kenwood) |
| [JCTVC-H0278](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4581) | Non-CE9: CU-based parallel merge mode | J.-L. Lin, Y.-W. Chen, Y.-W. Huang, S. Lei (MediaTek) |
|  |  |  |
| [JCTVC-H0087](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4388) | Non-CE9: Cross-verification of removing PU dependency in TMVP reference index derivation (JCTVC-H0092 from LGE and Qualcomm) | [M. Zhou (](mailto:zhou@ti.com)TI) |
| [JCTVC-H0093](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4394) | Non-CE9: Crosscheck of Panasonic's proposal on TMVP refIdx derivation in merge/skip (JCTVC-H0214) | [Y. Jeon](mailto:yongjoon.jeon@lge.com), [B. Jeon (LG](mailto:bm.jeon@lge.com)) |
| [JCTVC-H0218](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4521) | Non-CE9: Cross-check report of JVC KENWOOD’s modified derivation process of the reference index for temporal merging candidate (JCTVC-H0199) by Panasonic | [T. Sugio](mailto:sugio.toshiyasu@jp.panasonic.com), T. Nishi (Panasonic) |
| [JCTVC-H0592](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4906) | Non-CE9: Cross-verification of JCTVC-H0278 on CU-based parallel merge mode | V. Seregin, X. Wang, J.Chen (Qualcomm) |

Another category of CU-level parallel merge/skip is aimed to reduce the number of MCLs. It is proposed to derive MCL for a CU only once and the same MCL is shared by all the PUs inside the CU. The following contribution enable CU level of parallel merge/skip with the number of MCLs is reduced to 1/7 of HM5.

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| Document | Title | Proponents |
| [JCTVC-H0240](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4543) | Non-CE9: Throughput improvement for merge/skip mode | [H. Y. Kim (ETRI)](mailto:hykim5@etri.re.kr), [K. Y. Kim](mailto:kimky@khu.ac.kr), [S. M. Kim](mailto:jephiros@khu.ac.kr), [G. H. Park (KHU)](mailto:ghpark@khu.ac.kr), [S.-C. Lim](mailto:sclim@etri.re.kr), [J. Lee](mailto:jinosoul@etri.re.kr), [S. Cho](mailto:shcho@etri.re.kr), [J. S. Choi (ETRI)](mailto:jschoi@etri.re.kr) |
| [JCTVC-H0629](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4949) | Non-CE9: cross-check of H0240 on throughput improvement for merge/skip mode | P. Onno (Canon) |

SCU-level parallel merge/skip designed to remove inter-dependency of MCL derivation for the second, third and fourth PUs in a SCU of PART\_NxN mode. It is proposed to drop the neighboring PUs of a same SCU from the MCL derivation process.



**Figure 5. Cases when a PU has dependency with other PUs in the same CU in the spatial merging candidate derivation process for NxN partition mode [from JCTVC-H0091].**

The following contributions enable SCU level of parallel merge/skip (tests done for SCU size 8x8 only)

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| Document | Title | Proponents |
| [JCTVC-H0091](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4392) | Non-CE9: Parallel Merge Candidate Derivation for Inter\_NxN partition type | [Y. Jeon](mailto:yongjoon.jeon@lge.com), [B. Jeon (LG)](mailto:bm.jeon@lge.com), [V. Seregin](mailto:vseregin@qualcomm.com), [X Wang](mailto:xianglin@qualcomm.com), [J. Chen](mailto:cjianle@qualcomm.com), [M. Karczewicz (Qualcomm)](mailto:martak@qualcomm.com) |
| [JCTVC-H0219](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4522) | Non-CE9: Cross-check report of parallel merge candidate derivation for Inter\_NxN partition type (JCTVC-H0091) by Panasonic | [T. Sugio](mailto:sugio.toshiyasu@jp.panasonic.com), T. Nishi (Panasonic) |

The following contributions are related to the non-normative encoder speedup of the RD cost estimation for the MERGE/Skip candidate list.

|  |  |  |
| --- | --- | --- |
| Document | Title | Proponents |
| [JCTVC-H0178](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4477) | Encoder speed-up for the MV cost estimation | [G. Laroche](mailto:guillaume.laroche@crf.canon.fr), T. Poirier, [P. Onno (Canon)](mailto:patrice.onno@crf.canon.fr) |
| [JCTVC-H0241](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4477) | Cross-check report for Canon's encoder speed-up for the MV cost estimation (JCTVC-H0178) | [S.-C. Lim](mailto:sclim@etri.re.kr), [H. Y. Kim](mailto:hykim5@etri.re.kr), [J. Lee (ETRI)](mailto:jinosoul@etri.re.kr) |

**Related to mandate 4:**

The simulation results are reported as follows.

**Quantifying HM5 quality loss in PME environment for architecture HM5 PME, HM5 PME A and HM5 PME B.**

|  |  |  |
| --- | --- | --- |
| Document | Tools | Results (relative to HM5.0 anchor) |
| [JCTVC-H0082](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4383) | HM5 PME  (skip merge ME for affected PUs/CUs) | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **PME level** | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | 64 x 64 | 7.3 | 8.4 | 8.4 | 10.9 | | 32 x 32 | 5.3 | 6.3 | 6.6 | 8.4 | | 16 x 16 | 2.5 | 3.1 | 3.1 | 4.2 | | 8 x 8 | 0.2 | 0.3 | 0.3 | 0.4 | |
| [JCTVC-H0010](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4383) | \*HM5 PME A  (TMVP refIdx =0, skip merge ME for affected PUs/CUs) | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **PME level** | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | 64 x 64 | 7.1 | 8.3 | 8.2 | 10.8 | | 32 x 32 | 4.9 | 6.0 | 6.1 | 8.1 | | 16 x 16 | 2.0 | 2.7 | 2.5 | 3.6 | | 8 x 8 | 0.0 | 0.0 | 0.1 | 0.1 | |
| [JCTVC-H0010](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4383) | \*HM5 PME B  (TMVP refIdx = 0, partial merge ME for affected PUs/CUs, merge\_idx matching) | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **PME level** | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | 64 x 64 | 5.7 | 6.5 | 6.4 | 8.5 | | 32 x 32 | 3.5 | 4.3 | 4.0 | 5.5 | | 16 x 16 | 1.1 | 1.7 | 1.3 | 2.1 | | 8 x 8 | 0.0 | 0.0 | 0.1 | 0.1 | |

\*HM5 PME A and B results pending on cross-check from Qualcomm and other companies.

**CU-group level parallel skip/merge**

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| --- | --- | --- |
| Document | Tools | Results (relative to HM5.0 anchor) |
| [JCTVC-H0082](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4383) | Discarding MVPs from MCL if unavailable | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **PME level** | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | 64 x 64 | 2.6 | 3.3 | 3.4 | 4.7 | | 32 x 32 | 1.6 | 2.1 | 1.9 | 2.7 | | 16 x 16 | 0.5 | 0.8 | 0.5 | 0.9 | | 8 x 8 | 0.0 | 0.0 | 0.0 | 0.0 | |
| [JCTVC-H0090](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4391) | Replacing unavailable MVPs with the closest ones outside the MER | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **PME level** | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | 64 x 64 | 1.6 | 2.0 | 2.3 | 2.9 | | 32 x 32 | 0.9 | 1.1 | 1.1 | 1.5 | | 16 x 16 | 0.3 | 0.4 | 0.2 | 0.3 | | 8 x 8 | 0.0 | 0.0 | 0.0 | 0.0 | |

**CU-level parallel skip/merge (except for SCUs of PART\_NxN mode)**

|  |  |  |
| --- | --- | --- |
| Document | Tools | Results (relative to HM5.0 anchor) |
| [JCTVC-H0092](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4393) | 1. Fixing refIdx to zero 2. PUs of a CU share a same refIdx | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | refIDX=0 | 0.0 | 0.0 | 0.1 | 0.1 | | CU-based | 0.0 | 0.0 | 0.0 | 0.0 | |
| [JCTVC-H0214](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4517) | RefIdxLX = Min( refIdxCol, num\_ref\_idx\_lX\_active\_minus1 ) | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | refIdxCol | 0.0 | 0.0 | -0.1 | -0.1 | |
| [JCTVC-H0199](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4501) | 1. 2NxN left, Nx2N upper 2. 1st PU left, 2nd PU fixed to 0 3. Fixed to 0 | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | Propsoal1 | 0.0 | 0.0 | 0.0 | 0.0 | | Proposal2 | 0.0 | 0.0 | 0.0 | 0.0 | | Proposal3 | 0.0 | 0.0 | 0.1 | 0.1 | |
| [JCTVC-H0278](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4581) | 1st PU left, 2nd PU fixed to 0 | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | Proposed | 0.0 | 0.0 | 0.0 | 0.0 | |
| [JCTVC-H0240](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4543) | Variant1: PUs of a CU share a same TMVP refIdx (Identical to JCTVC-H0092) | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | Variant1 | 0.0 | 0.0 | 0.0 | 0.0 | |

**CU-level parallel skip/merge with reduced MCLs (except for SCUs of PART\_NxN mode)**

|  |  |  |
| --- | --- | --- |
| Document | Tools | Results (relative to HM5.0 anchor) |
| [JCTVC-H0240](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4543) | All PUs of a CU share a same MCL  1.     Original: all CUs  2.     Variant2: 8x8 CUs only | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | Original | 0.3 | 0.2 | 0.5 | 0.4 | | Variant2 | 0.1 | 0.1 | 0.2 | 0.2 | |

**SCU-level parallel skip/merge (results for 8x8 SCUs only)**

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| --- | --- | --- |
| Document | Tools | Results (relative to modified HM5.0 anchor) |
| [JCTVC-H0091](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4392) | exclude the MVPs located in a previous PU in the same CU | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | proposed | 0.0 | 0.1 | 0.0 | 0.0 | |

**Encoder merge/skip speedup**

|  |  |  |
| --- | --- | --- |
| Document | Tools | Results (relative to HM5.0 anchor) |
| [JCTVC-H0178](http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=4477) | Simplified RD estimation for merge/skip candidates (5% encoder runtime reduction) | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | proposed | 0.0 | 0.1 | 0.0 | 0.1 | |

**Related to mandate 5:**

A unified solution JCTVC-H0247 was submitted. JCTVC-H0247 basically is a harmonization of JCTVC-H0090, JCTVC-H0092 and JCTVC-H0240 with the following tools:

1. Single MCL for 8x8 CUs at all parallel merge levels (8x8, 16x16, 32x32 and 64x64) for number of MCL reduction
2. Decoupling of MCL derivation process from the regular ME at all parallel merge levels by replacing unavailable MVPs with the closet ones outside the parallel ME region in the MCL derivation process
3. CUs above parallel merge block level shares a same reference index for TMVP (CU-level parallel merge/skip)
4. A slice-level flag to signal parallel merge/skip level and offer option of disabling tool 1 & 2.

|  |  |  |
| --- | --- | --- |
| Document | Tools | Results (relative to HM5.0 anchor) |
| JCTVC-H0247 | 1. Single MCL for 8x8 CUs 2. CU-group level MCL decoupling 3. CU-level TMVP refIdx 4. Parallel level signaling | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **PME level** | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | 64 x 64 | 1.7 | 2.0 | 2.3 | 3.1 | | 32 x 32 | 0.9 | 1.2 | 1.2 | 1.6 | | 16 x 16 | 0.3 | 0.5 | 0.4 | 0.6 | | 8 x 8 | 0.1 | 0.2 | 0.2 | 0.3 | |

As reference, JCTVC-H0082 section 6 reports the combined study results on unified design with JCTVC-H0092 and JCTVC-H0240 with the following tools:

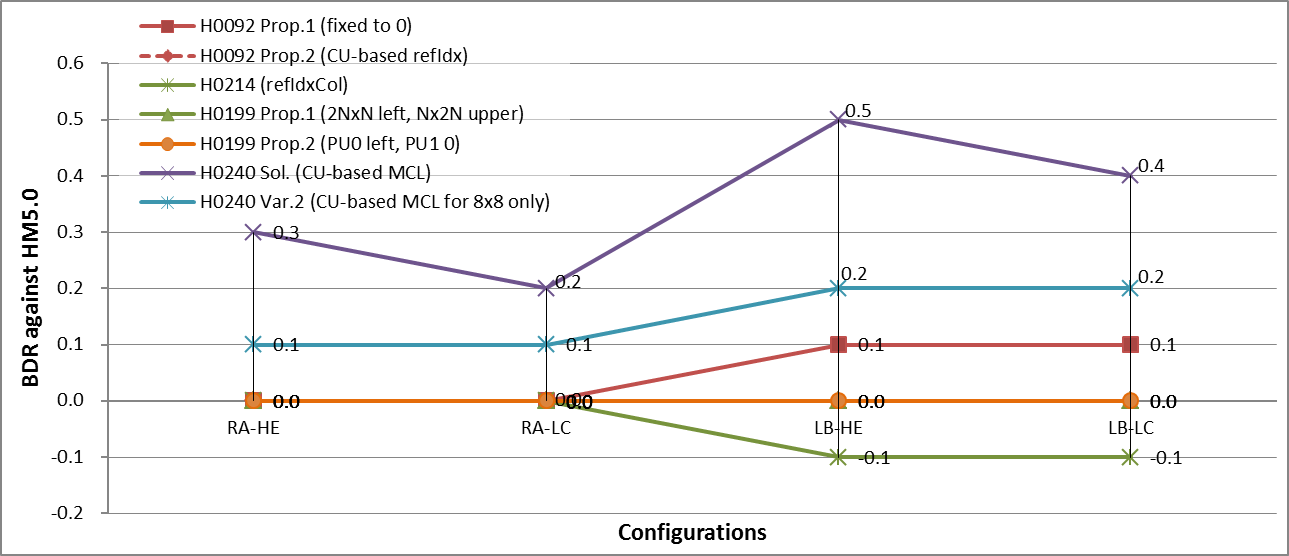
1. Single MCL for 8x8 CUs at all parallel merge levels (8x8, 16x16, 32x32 and 64x64) for number of MCL reduction
2. Decoupling of MCL derivation process from the regular ME at all parallel merge levels by excluding unavailable MVPs from the MCL derivation process
3. Fixing TMVP reference index to 0 (CU-level parallel merge/skip)
4. A picture-level flag to signal parallel merge/skip level and offer option of disabling tool 1 & 2.

|  |  |  |
| --- | --- | --- |
| Document | Tools | Results (relative to HM5.0 anchor) |
| JCTVC-H0082 section 6 | 1. Single MCL for 8x8 CUs 2. CU-group level MCL decoupling 3. TMVP refIdx = 0 4. Parallel level signaling | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **PME level** | **RA-HE (%)** | **RA-LC (%)** | **LB-HE (%)** | **LB-LC (%)** | | 64 x 64 | 2.7 | 3.3 | 3.4 | 4.8 | | 32 x 32 | 1.6 | 2.2 | 2.0 | 2.8 | | 16 x 16 | 0.6 | 0.9 | 0.7 | 1.1 | | 8 x 8 | 0.1 | 0.1 | 0.2 | 0.3 | |

**Summary of the results**

The following table and Figure 6 summarize the BDR results of CU-level PME proposals.

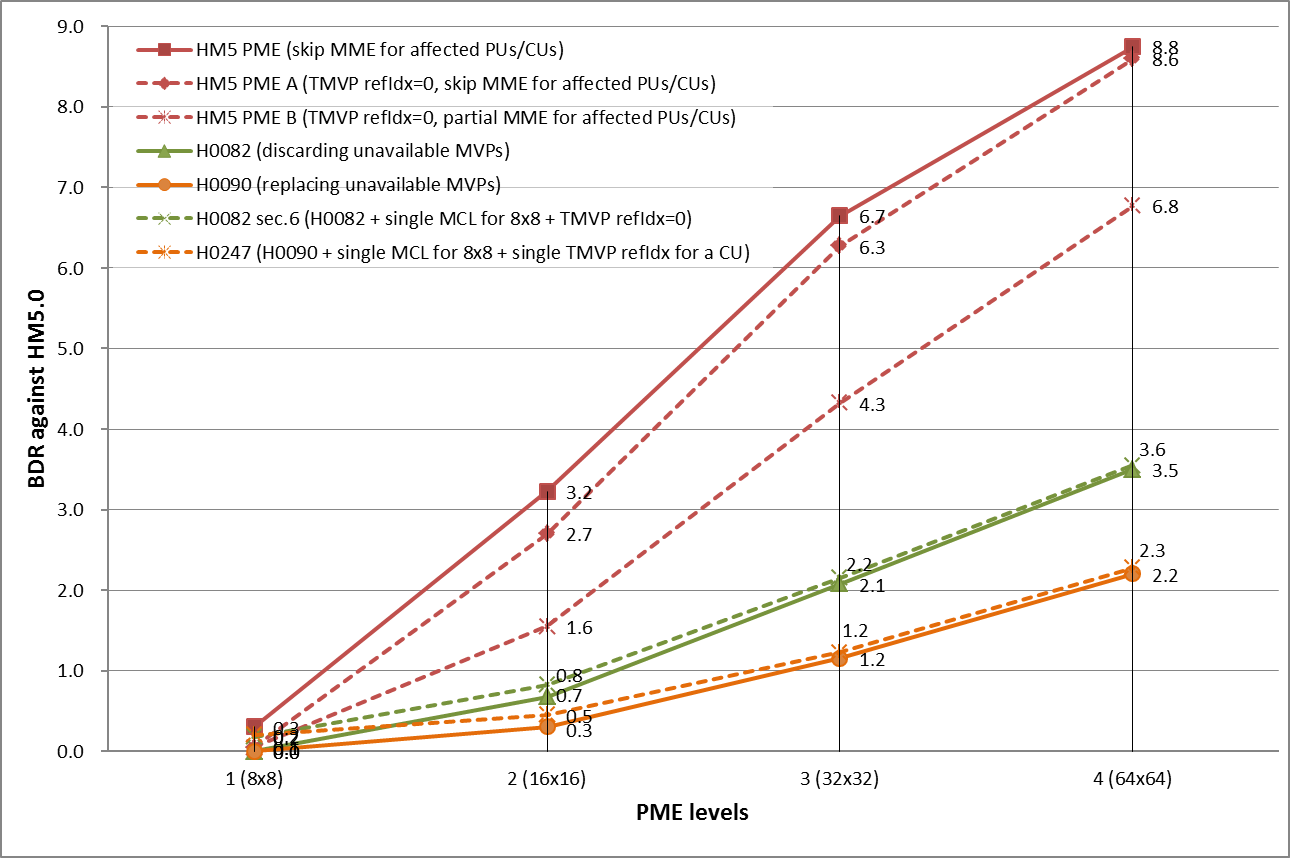
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Category** | **Tool** | **Identical to** | **RA-HE** | **RA-LC** | **LB-HE** | **LB-LC** | **Average** |
| **TMVP refIdx dependency removal** | **H0092 Prop.1** (fixed to 0) | **H0199 Prop.3** | 0.0 | 0.0 | 0.1 | 0.1 | **0.1** |
| **H0092 Prop.2** (CU-based refIdx) | **H0240 Var.1** | 0.0 | 0.0 | 0.0 | 0.0 | **0.0** |
| **H0214** (refIdxCol) | **-** | 0.0 | 0.0 | -0.1 | -0.1 | **-0.1** |
| **H0199 Prop.1** (2NxN left, Nx2N upper) | **-** | 0.0 | 0.0 | 0.0 | 0.0 | **0.0** |
| **H0199 Prop.2** (PU0 left, PU1 0) | **H0278** | 0.0 | 0.0 | 0.0 | 0.0 | **0.0** |
| **With reduced MCLs** | **H0240 Sol.** (CU-based MCL) | **-** | 0.3 | 0.2 | 0.5 | 0.4 | **0.4** |
| **H240 Var.2** (CU-based MCL for 8x8 only) | **-** | 0.1 | 0.1 | 0.2 | 0.2 | **0.2** |



**Figure 6. BDR comparison of CU-level PME tools.**

The following table and Figure 7 summarize the BDR results of CU-group level PME proposals.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Category** | **Tool** | **PME level** | | | |
| **1 (8x8)** | **2 (16x16)** | **3 (32x32)** | **4 (64x64)** |
| **HM5 PMEs** | **HM5 PME** (skip MME for affected PUs/CUs) | 0.3 | 3.2 | 6.7 | 8.8 |
| **HM5 PME A** (TMVP refIdx=0, skip MME for affected PUs/CUs) | 0.1 | 2.7 | 6.3 | 8.6 |
| **HM5 PME B** (TMVP refIdx=0, partial MME for affected PUs/CUs) | 0.1 | 1.6 | 4.3 | 6.8 |
| **CU-Group level PMEs** | **H0082** (discarding unavailable MVPs) | 0.0 | 0.7 | 2.1 | 3.5 |
| **H0090** (replacing unavailable MVPs) | 0.0 | 0.3 | 1.2 | 2.2 |
| **Combined with H0240 and H0092** | **H0082 sec.6** (H0082 + single MCL for 8x8 + TMVP refIdx=0) | 0.2 | 0.8 | 2.2 | 3.6 |
| **H0247** (H0090 + single MCL for 8x8 + single TMVP refIdx for a CU) | 0.2 | 0.5 | 1.2 | 2.3 |



**Figure 7. BDR comparison of CU-group level PME tools.**

# Recommendations

Review the related contributions.