Non-CE9: Division-free MV scaling

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Overall Summary

- Double the effective scaling range to deal with the reference pictures of longer temporal distances
  - Ref. frame setting in low delay: 1 nearest reference frame and 3 high quality reference frames (JCTVC-F701)
  - Reduce 0.1% of bit rate in low delay cases

- A division-free MV scaling
  - Replace the general divider by a small look-up table and simple arithmetic operations
  - Reduce 54-58% of gate count in MV scaling module without bit rate increase

	HE-RA	LC-RA	HE-LDB	LC-LDB	HE-LDP	LC-LDP
2X scaling range	0.0%	0.0%	-0.1%	-0.1%	-0.1%	-0.1%
Division-free	0.0%	0.0%	-0.1%	-0.1%	-0.1%	-0.1%

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MV Scaling in HM-4.0

1. Derive the *ScaleFactor*

$$ScaleFactor = \frac{POC_{curr} - POC_{ref}}{POC_{col} - POC_{col\_ref}} = \frac{TDB}{TDD}$$

$$tX = \frac{2^{14} + \left| \frac{TDD}{2} \right|}{TDD} \quad \Leftarrow \text{Divider}$$

$$ScaleFactor = clip(-1024, 1023, (TDB \times tX + 32) >> 6)$$

2. Derive the *scaledMV* **Effective scaling range is [-4,4)**

$$ScaledMV = sign(ScaleFactor \times MV) \times$$
$$(abs(ScaleFactor \times MV) + 127)) >> 8)$$

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Double the Effective Scaling Range

- Scaling range of [-4,4) is not enough in low delay cases
  - JCTVC-F701 : 1 nearest reference frame and 3 high quality reference frames
  - Scale ratio may be outside the range of [-4,4) easily
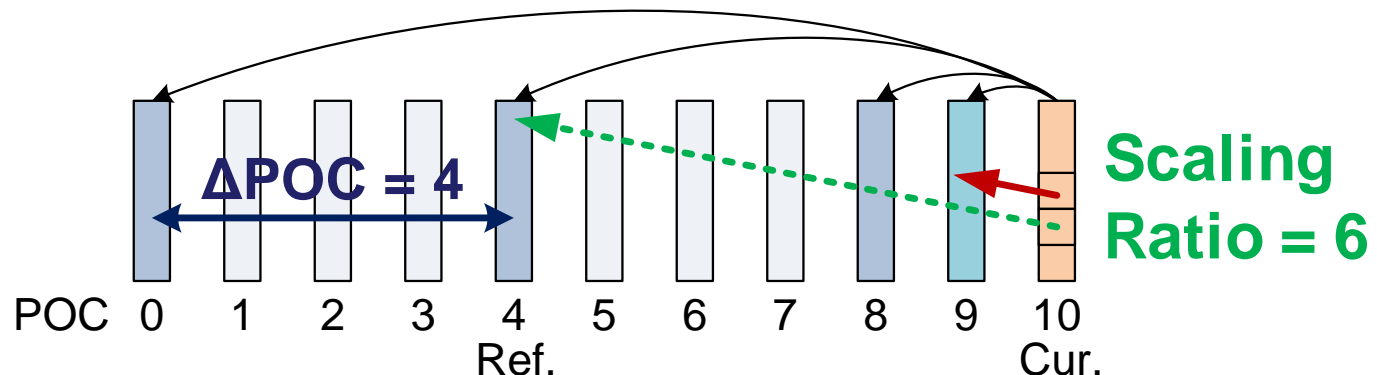
- Double the effective scaling range, [-4,4) → [-8,8)
  - $ScalingFactor = clip (\textbf{-1024, 1023}, (tbxtX+32)>>6)$
  - $ScalingFactor = clip (\textbf{-2048, 2047}, (tbxtX+32)>>6)$

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Result –Enlarged Effective Scaling Range

- Enlarged effective scaling range ([-4,4) → [-8,8))

- 0.1% of bit rate reduction

- No additional gain for the scaling range of [-16,16)

	Random Access HE			Low delay B HE			Low delay P HE		
	Y	U	V	Y	U	V	Y	U	V
Class A	0.0%	0.0%	0.0%						
Class B	0.0%	0.0%	0.0%	-0.2%	-0.4%	-0.3%	-0.1%	-0.2%	0.1%
Class C	0.0%	0.0%	0.0%	-0.1%	-0.1%	0.0%	-0.1%	-0.2%	-0.1%
Class D	0.0%	0.0%	0.0%	-0.1%	-0.1%	-0.1%	0.0%	0.0%	-0.1%
Class E				0.0%	0.2%	0.2%	0.0%	-0.2%	0.2%
Overall	**0.0%**	**0.0%**	**0.0%**	**-0.1%**	**-0.2%**	**-0.1%**	**-0.1%**	**-0.2%**	**0.0%**
	0.0%	0.0%	0.0%	-0.1%	-0.2%	-0.1%	-0.1%	-0.2%	0.0%
Enc Time[%]		100%			99%			99%	
Dec Time[%]		100%			100%			100%	

	Random Access LC			Low delay B LC			Low delay P LC		
	Y	U	V	Y	U	V	Y	U	V
Class A	0.0%	0.0%	0.0%						
Class B	0.0%	0.0%	0.0%	-0.1%	-0.3%	-0.2%	-0.2%	-0.1%	-0.7%
Class C	0.0%	0.0%	0.0%	-0.1%	-0.1%	-0.2%	-0.1%	0.0%	-0.1%
Class D	0.0%	0.0%	0.0%	0.0%	0.1%	-0.2%	-0.1%	-0.2%	-0.2%
Class E				-0.1%	0.2%	0.1%	0.0%	-0.3%	-0.2%
Overall	**0.0%**	**0.0%**	**0.0%**	**-0.1%**	**-0.1%**	**-0.1%**	**-0.1%**	**-0.1%**	**-0.3%**
	0.0%	0.0%	0.0%	-0.1%	-0.1%	-0.1%	-0.1%	-0.1%	-0.4%
Enc Time[%]		100%			100%			99%	
Dec Time[%]		101%			100%			100%	

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HW Circuit Diagram of MV Scaling Module in HM-4.0

- One divider is required for MV scaling

- **The divider is undesirable in HW implementation**
  - Divider occupies over 60% of gate counts in the MV scaling module

- Try to replace the divider with small look-up table and simple arithmetic operations

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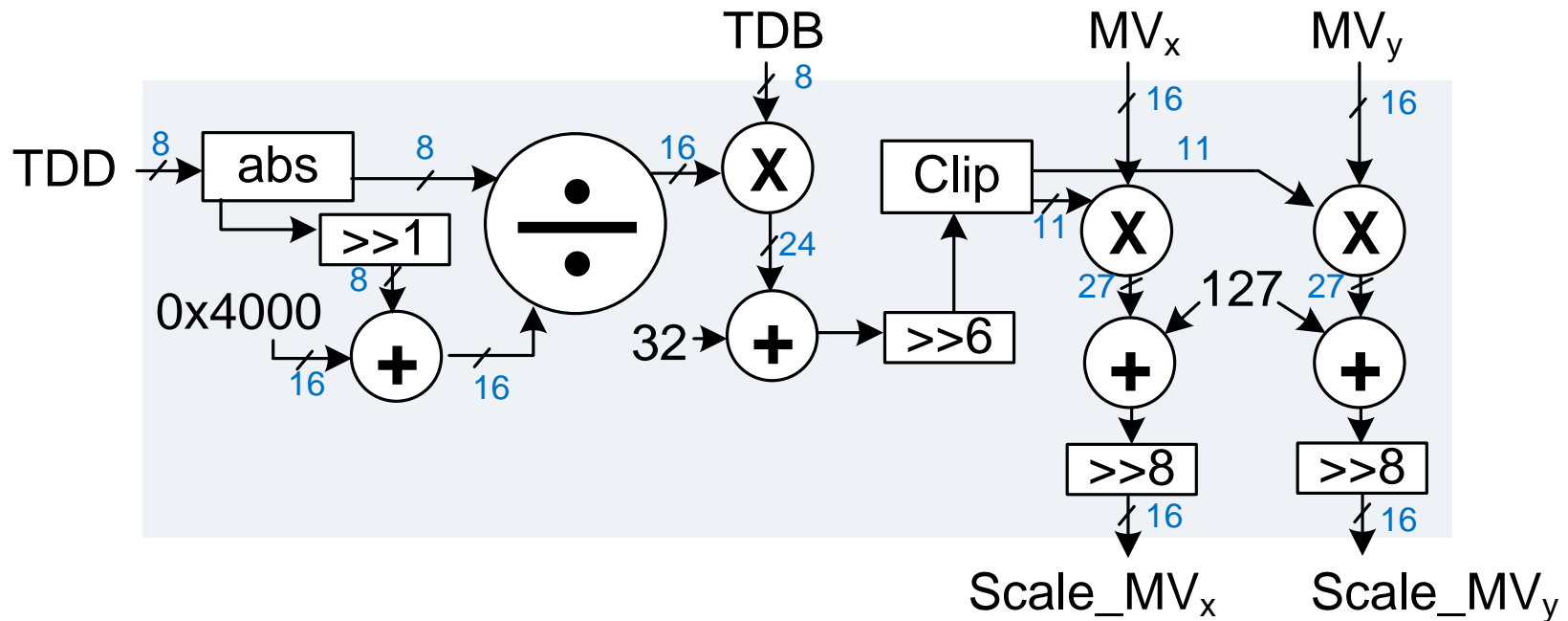
Proposed Division-free MV Scaling (1)

1. Use a small look-up table to derive *128/TDD (the tX)*

$$If\,(TDD<16)$$
$$tX = 128\_div\_TDD[TDD]$$
$$Else$$
$$tX = 128\_div\_TDD[TDD>>n]$$

TDD	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
128_div_TDD	128	64	43	32	26	21	18	16	14	13	12	11	10	9	8

$\frac{128}{1}$ $\frac{128}{2}$ $\frac{128}{3}$ $\frac{128}{4}$ $\frac{128}{5}$ $\frac{128}{6}$ $\frac{128}{7}$ $\frac{128}{8}$ $\frac{128}{9}$ $\frac{128}{10}$ $\frac{128}{11}$ $\frac{128}{12}$ $\frac{128}{13}$ $\frac{128}{14}$ $\frac{128}{15}$

$$\frac{128}{16} = \frac{128}{8}>>1 \qquad \frac{128}{17} \approx \frac{128}{8}>>1$$

2. Derive *ScaleFactor*

$$ScaleFactor = clip(-1024,1023,(TDB \times tX)>>n)$$

Proposed Division-free MV Scaling (2)

3. Derive *ScaledMV*

$$ScaledMV = sign(ScaleFactor \times MV) \times$$

$$(abs(ScaleFactor \times MV) + 63)) >> 7)$$

HW Circuit Diagram of Proposed MV Scaling Module

- Division-free MV scaling
  - *n* is the position of the first "1" of binarized TDD
    - Can be implemented with a few bits of comparators and MUX
    - No look-up table is required for n

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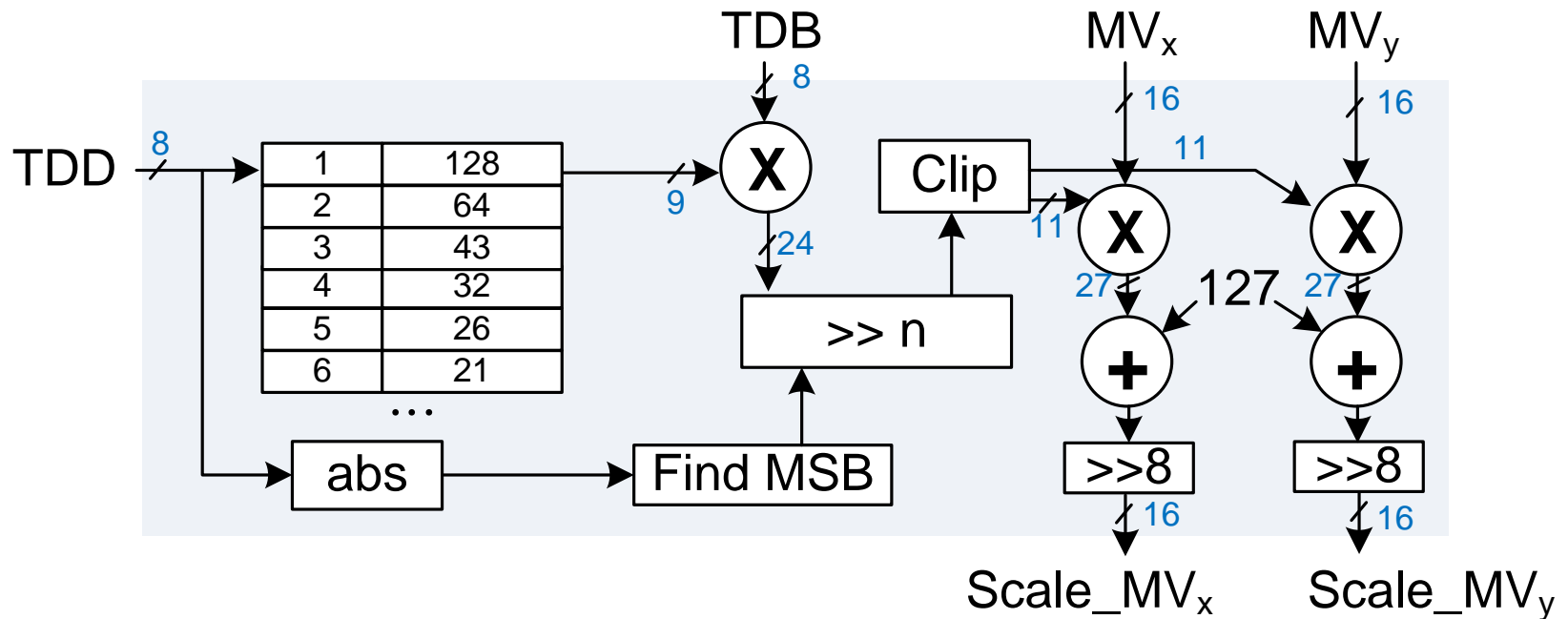
Hardware Synthesis Result

- Implemented with Verilog

- TSMC 40nm Process, Synopsis Design Compiler

- 54-58% of gate count is reduced

200 MHz	Gate counts	Reduction	Latency
HM-4.0	7,331	–	0 cycle
Proposed	3,093	58%	0 cycle

300 MHz	Gate counts	Reduction	Latency
HM-4.0 (pipelined)	7,250	–	1 cycle
Proposed	3,349	54%	0 cycle

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Result

- 0.1% of bit rate reduction in low delay cases

- No loss compared to enlarged effective scaling range

	Random Access HE			Low delay B HE			Low delay P HE		
	Y	U	V	Y	U	V	Y	U	V
Class A	0.0%	-0.2%	-0.2%						
Class B	0.0%	0.1%	0.0%	-0.2%	-0.1%	-0.1%	-0.2%	0.0%	0.0%
Class C	0.0%	0.0%	0.1%	-0.1%	-0.1%	-0.3%	0.0%	-0.1%	-0.1%
Class D	0.0%	-0.1%	0.0%	0.0%	0.1%	0.2%	0.0%	-0.2%	-0.3%
Class E				0.0%	0.4%	0.3%	-0.1%	-0.4%	-0.2%
Overall	**0.0%**	**0.0%**	**0.0%**	**-0.1%**	**0.0%**	**0.0%**	**-0.1%**	**-0.2%**	**-0.1%**
	0.0%	0.0%	0.0%	-0.1%	0.0%	0.0%	-0.1%	-0.2%	-0.2%
Enc Time[%]	100%			99%			99%		
Dec Time[%]	99%			99%			99%		

	Random Access LC			Low delay B LC			Low delay P LC		
	Y	U	V	Y	U	V	Y	U	V
Class A	0.0%	0.1%	0.1%						
Class B	0.0%	0.0%	0.0%	-0.1%	-0.1%	-0.2%	-0.2%	-0.1%	-0.2%
Class C	0.0%	0.0%	-0.1%	-0.1%	0.1%	-0.3%	-0.1%	-0.1%	-0.1%
Class D	0.0%	-0.1%	0.0%	0.0%	0.1%	0.4%	-0.1%	-0.3%	-0.4%
Class E				-0.1%	-0.3%	0.3%	0.0%	-0.2%	0.1%
Overall	**0.0%**	**0.0%**	**0.0%**	**-0.1%**	**0.0%**	**0.0%**	**-0.1%**	**-0.2%**	**-0.2%**
	0.0%	0.0%	0.0%	-0.1%	-0.1%	0.0%	-0.1%	-0.2%	-0.2%
Enc Time[%]	100%			99%			99%		
Dec Time[%]	99%			100%			100%		

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Cross Verification

- We thank Canon for crosschecking our proposal
  - JCTVC-G523

- BD-rates and run times are confirmed

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Conclusions

- Propose to double the effective scaling range
  - Reduce 0.1% of bit rate in low delay cases

- Proposed a division-free MV scaling
  - Replace the general divider by a small look-up table and simple arithmetic operations
  - Reduce 54-58% of gate count of MV scaling module without bit rate increase

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Thank You.

Use Large Look-up Table for Division

- The divider can be replaced with a 256x16bits look-up table
- Proposed : 31x9 bits table, 93% of table size reduction
- 31% of gate count reduction

300 MHz	Gate counts	Reduction	Latency
HM-4.0 table	4,836	–	0 cycle
Proposed	3,349	31%	0 cycle

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