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AHG4: Low latency CABAC initialization for dependent tiles

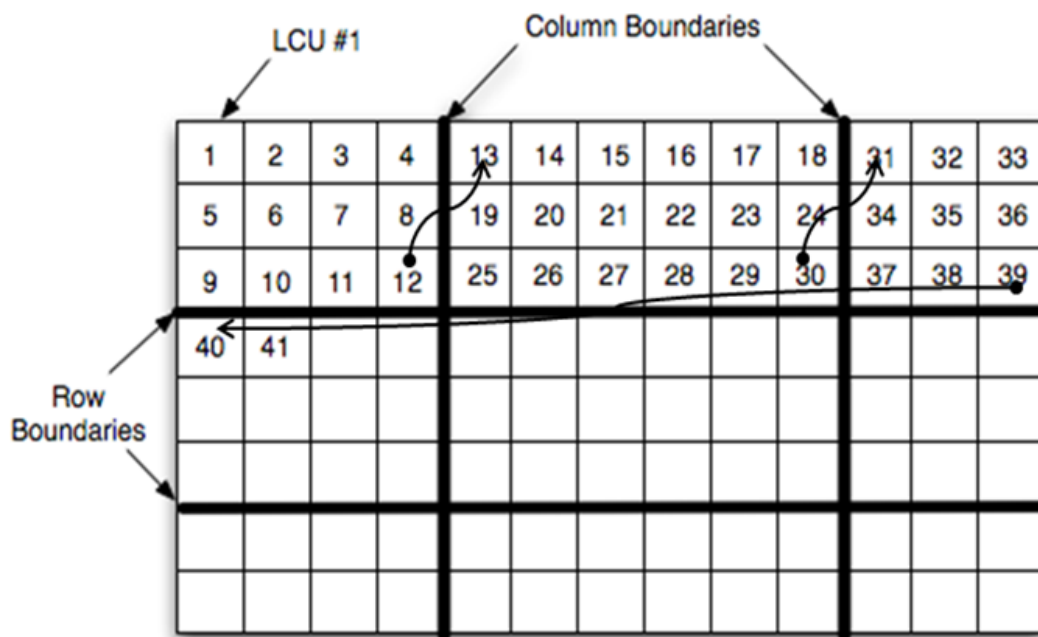Chih-Wei Hsu, Chia-Yang Tsai, Yu-Wen Huang, Shawmin Lei

Overall Summary

- In this contribution, low latency CABAC initialization for dependent tiles is proposed
  - CABAC probabilities of the first LCU in each tile are inherited from those of the adjacent left LCU

- The proposed method is compared with dependent tiles of HM-4.0-dev
  - 0-0.2% and 0-0.7% bit rate increases when the number of tile columns is two and four
  - The processing latency for non-first column tiles is reduced from almost one picture to at most one LCU row

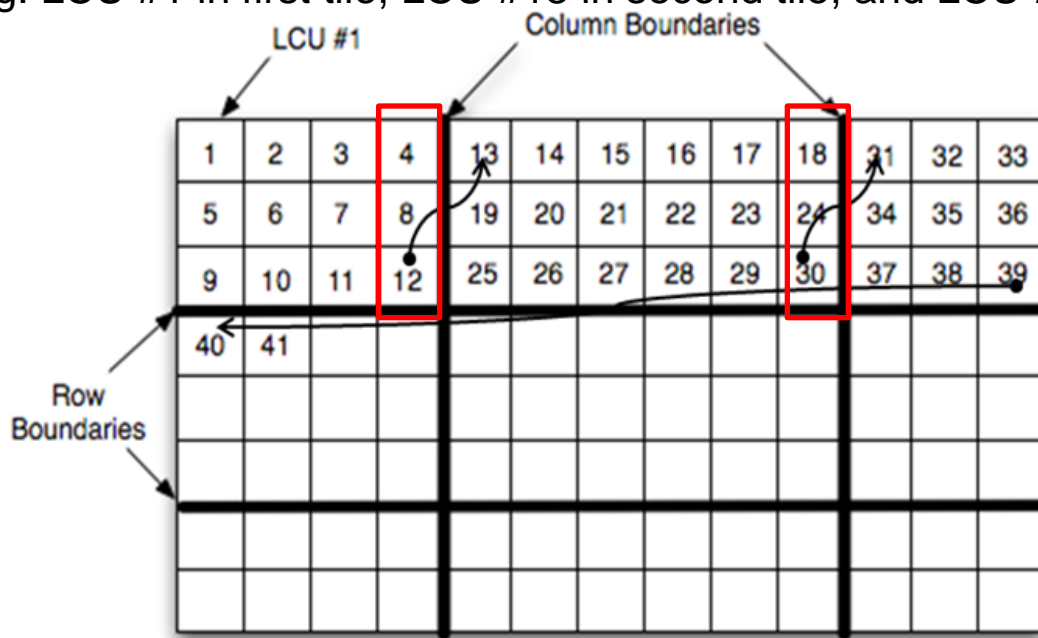**MEDIATEK**

Problem Definition

- Dependent tiles are processed using tile structure scan order and are allowed to use data from neighboring tiles

- The CABAC inheritance also follows that order
  - CABAC probabilities for LCU #13 will inherit from those of LCU #12, CABAC probabilities for LCU #31 will inherit from those of LCU #30, and so on

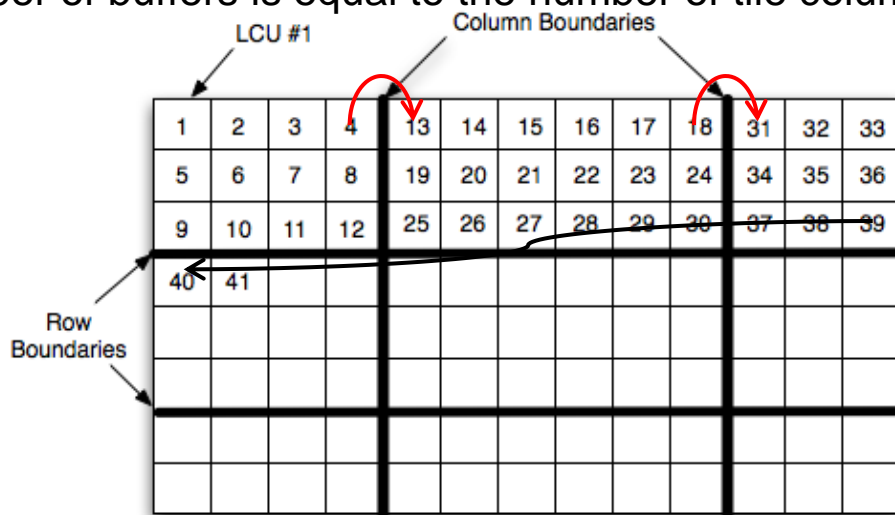Dependent tiles with three columns and three rows

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Problem Definition (Cont'd)

- For low latency applications, one LCU row cannot be processed at a time
  - E.g. first LCU row: LCU #1-4, LCU #13-18, LCU #31-33

- For single core applications, extra LCU column buffers are demanded for storing coded information (reconstructed pixels, motion data, etc.)
  - E.g. LCU #4, #8, #12 for LCU #13, #19, #25

- For multi-core applications, tiles cannot be processed in parallel
  - E.g. LCU #1 in first tile, LCU #13 in second tile, and LCU #31 in third tile

Proposed Method

- CABAC probabilities of the first LCU in each tile are inherited from those of the adjacent left LCU
  - E.g. the CABAC probabilities of LCU #13 are inherited from those of LCU #4 instead of LCU #12, LCU #31 are inherited from LCU #18 instead of LCU #30

- When tile entry points can be provided to locate the current tile positions in the bitstream
  - Processing of the first LCU in different tiles can start as long as the left LCU has been processed

- Buffers are required to store the CABAC probabilities of the left LCU
  - The number of buffers is equal to the number of tile columns minus one

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Simulation Results

- Anchor: HM-4.0, no tile settings

- Dependent tiles in HM-4.0-dev and the proposed method were tested for two and four tile columns
  - 0-0.2% bit rate increase for 2 tile columns; 0-0.7% bit rate increase for 4 tile columns

2 tile columns

	HE-AI			HE-RA			HE-LD		
	Y	U	V	Y	U	V	Y	U	V
HM-4.0-dev	0.0	-0.5	-0.7	0.2	-0.6	-0.8	0.4	0.3	0.1
Proposed method	0.0	-0.4	-0.6	0.4	-0.4	-0.6	0.6	0.4	0.4

4 tile columns

	HE-AI			HE-RA			HE-LD		
	Y	U	V	Y	U	V	Y	U	V
HM-4.0-dev	0.0	-0.5	-0.7	0.2	-0.5	-0.8	0.3	0.2	-0.1
Proposed method	0.0	-0.3	-0.5	0.5	-0.0	-0.3	1.0	1.0	0.9

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Conclusions

- MediaTek proposed a low latency CABAC initialization method for dependent tiles

- The proposed method was compared with dependent tiles of HM-4.0-dev
  - 0-0.2% bit rate increase for 2 tile columns and 0-0.7% bit rate increase for 4 tile columns
  - The processing latency for non-first column tiles is reduced from almost one picture to at most one LCU row

- In current HM-4.0, entry points (tile locations and markers) are only allowed for independent tiles
  - It is also proposed to remove the constraint
  - Dependent tiles can use entry points to facilitate low latency parallel processing

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