

CE12 subset 2: Test results and architectural study on de-blocking filter without parallel on/off filter decision

JCTVC-G088

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Proposed changes

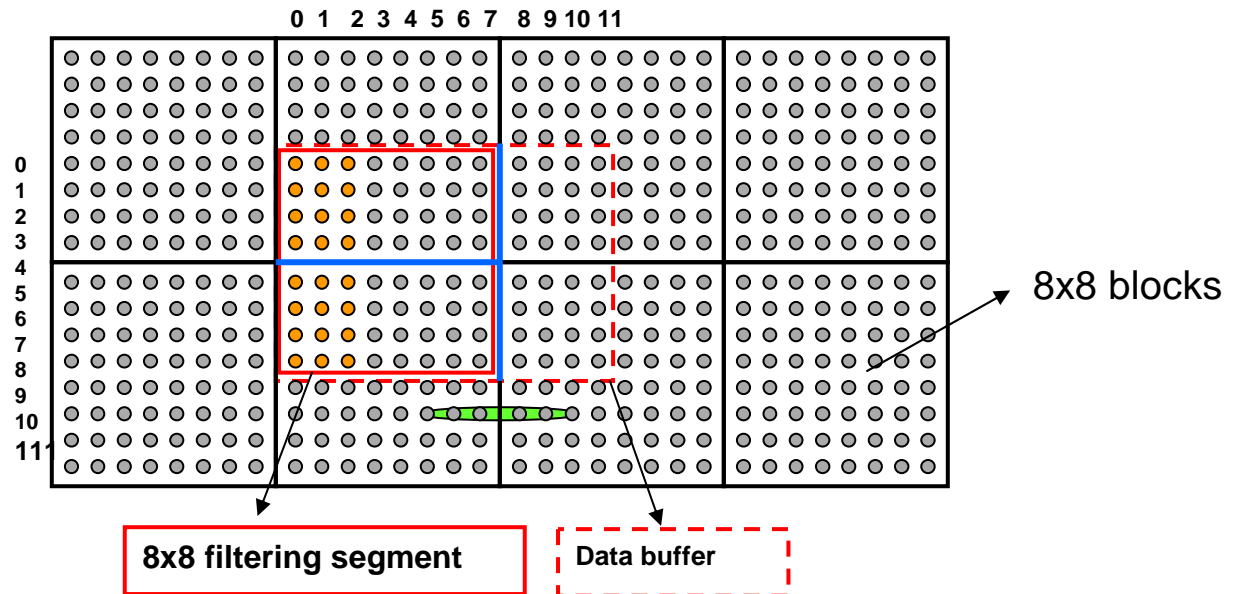
For de-blocking filter on/off decision (JCTVC-F256)

- Use un-filtered samples for on/off filter decision of vertical edges
- *Use the inter-mediate filtered samples (i.e. filtered samples after vertical edge filtering) for the on/off decision of horizontal edges*
 - **i.e. use the same input for both filter decision and filtering**

Major drawbacks of parallel on/off filter decision

1. It breaks a commonly used de-blocking filter architecture without intended benefits
 - In H.264/AVC de-blocking filter line buffer can store inter-mediate samples (i.e. filtered samples after vertical edge filtering)
 - This is no longer possible with the HM4.0 design w/o a significant increase of line buffer size
2. At micro architecture level, it was found that the parallel filter decision won't improve throughput
 - For a same HW cost (buffer size, memory reads and logic area) the parallel decision slows down the vertical edge filtering, because the vertical edge filtering cannot overwrite the data before the on/off decision on un-filtered samples for the horizontal edge is done.
 - For a same throughput six additional lines of un-filtered data will need to be loaded separately for the on/off filter decision of the horizontal edge. This increases both memory reads and buffer size.

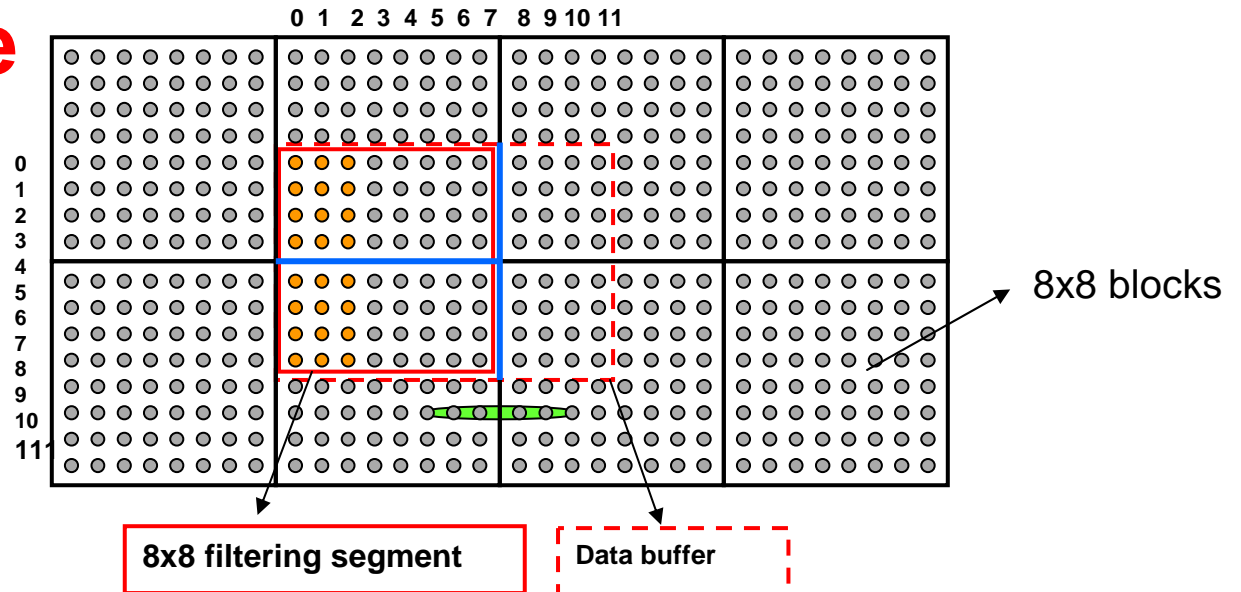
De-blocking filter architecture and assumptions



Assumptions

- Single-cycle 4x4 tile memory or 8 x2 line memory reads and writes
- Single-cycle filtering for a line or column
- Single-cycle filter on/off decision
- Single filter logic which is shared by horizontal and vertical edge filtering

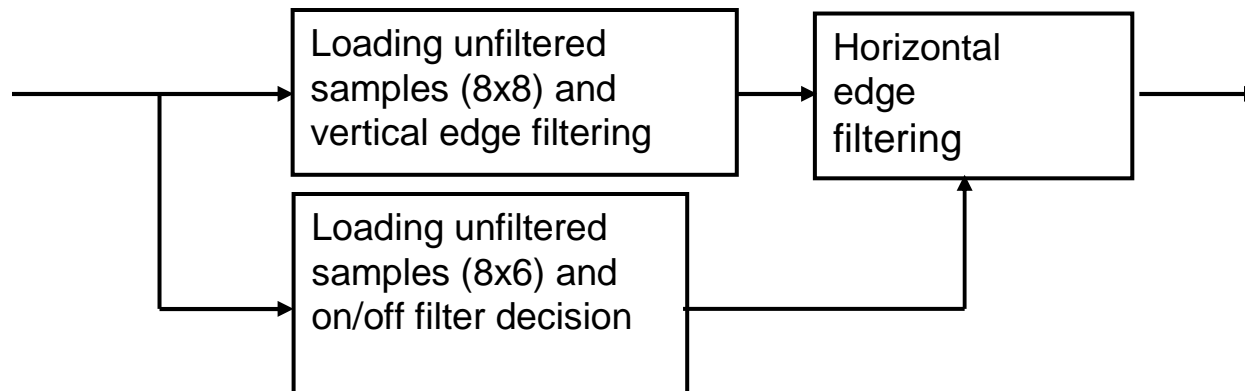
Cycle Estimate



For 4x4 tile memory format

Proposed (w/o parallel on/off decision)		HM4.0 (w/ parallel on/off decision)	
Operations	cycles	Operations	cycles
Load line 0 to 3	2	Load line 0 to 3	2
Load line 4 to 7, process line 0 & 1	2	Load line 4 to 7, process line 0	2
Load line 8 to 11, process line 2 & 3	2	Load line 8 ~ 11, horizontal on/off decision	2
Process line 4, vertical on/off decision	1	Process line 1, 2, 3, vertical edge on/off decision	3
Process line 5 & 6	2	Process line 4 to 7	4
Process line 7, horizontal on/off decision	1	Process column 0 to 7	8
Process column 0 to 7	8		
Store 8x8 samples	4*	Store 8x8 samples	4*
11/21/2011 Total	22		25

HM4.0 de-blocking architecture for a same throughput



- For each 8x8 filtering segment, six extra un-filtered sample lines (size 8 x 6, line 1 to 6) need to be loaded and buffered
 - Increased memory reads and data buffer size

Experimental results (1)

	All Intra HE			All Intra LC		
	Y	U	V	Y	U	V
Class A	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
Class B	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
Class C	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
Class D	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
Class E	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
Class F						
Overall	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
Enc Time[%]	100%			100%		
Dec Time[%]	100%			99%		

Experimental results (2)

	Random Access HE			Random Access LC		
	Y	U	V	Y	U	V
Class A	0.0%	-0.2%	-0.1%	0.0%	0.2%	0.0%
Class B	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%
Class C	0.0%	-0.1%	0.1%	0.0%	0.0%	-0.1%
Class D	0.0%	0.0%	0.0%	0.0%	-0.1%	0.0%
Class E						
Class F						
Overall	0.0%	-0.1%	0.0%	0.0%	0.0%	0.0%
	0.0%	-0.1%	0.0%	0.0%	0.0%	0.0%
Enc Time[%]	100%			100%		
Dec Time[%]	99%			96%		

Experimental results (3)

	Low delay B HE			Low delay B LC		
	Y	U	V	Y	U	V
Class A						
Class B	0.0%	0.0%	-0.2%	0.0%	0.0%	0.0%
Class C	0.0%	0.1%	0.0%	0.0%	0.2%	-0.2%
Class D	0.0%	0.4%	-0.3%	0.0%	0.2%	-0.2%
Class E	0.1%	0.0%	0.4%	0.0%	0.1%	-0.3%
Class F						
Overall	0.0%	0.1%	-0.1%	0.0%	0.1%	-0.1%
	0.0%	0.1%	-0.1%	0.0%	0.1%	-0.1%
Enc Time[%]	101%			100%		
Dec Time[%]	99%			99%		

Subjective viewing results

No visual difference was observed for all the CE12 selected visual testing sequences

Conclusions

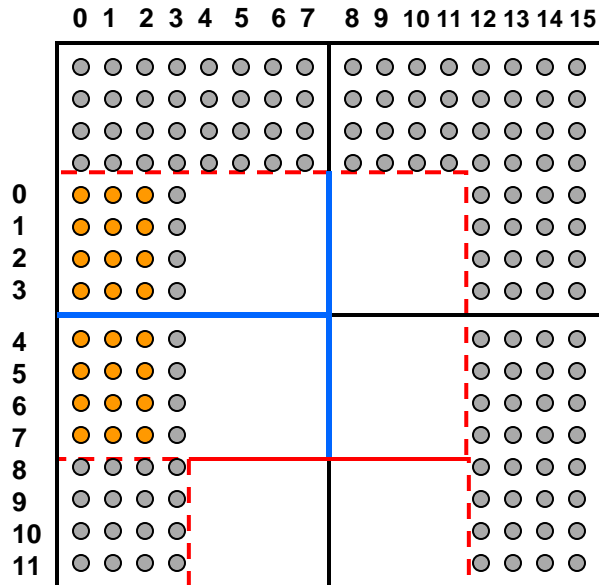
1. The current HM4.0 de-blocking filter design with parallel on/off filter decision does not have intended throughput benefits.
Instead, it breaks a commonly used de-blocking filter architecture which allows storing intermediate samples in line buffer
2. It is recommended to restore the AVC fashion of on/off filter decision
 - Use un-filtered samples for on/off filter decision of vertical edges
 - *Use the inter-mediate filtered samples (i.e. filtered samples after vertical edge filtering) for the on/off decision of horizontal edges*

Cross-checker: JCTVC-G588 (Panasonic), JCTVC-G746 (Samsung)

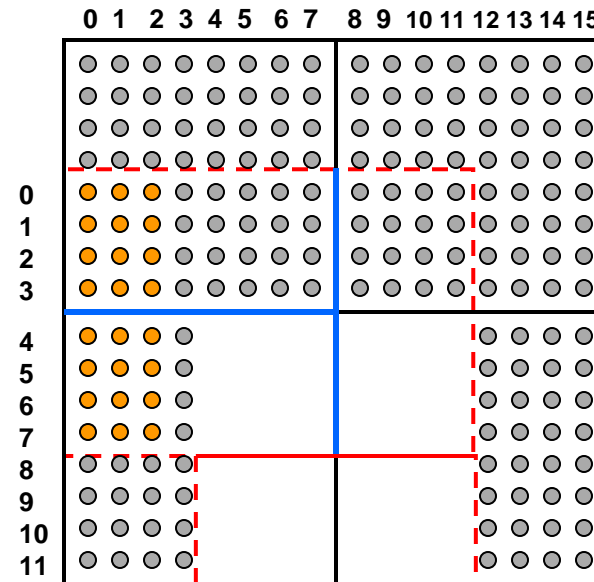
Cycle estimate for 4x4 tile memory format

- Architecture assumptions
 - Single-cycle 4x4 tile memory reads and writes
 - Single-cycle filtering for a line or column
 - Single-cycle filter on/off decision
 - Horizontal and vertical edge filtering shares a same logic
- Cycle count for 8x8 filtering area with same cost (cycle budget 50 cycles per 8x8)
 - w/o parallel decision 22 cycles
 - w/ parallel decision 25 cycles

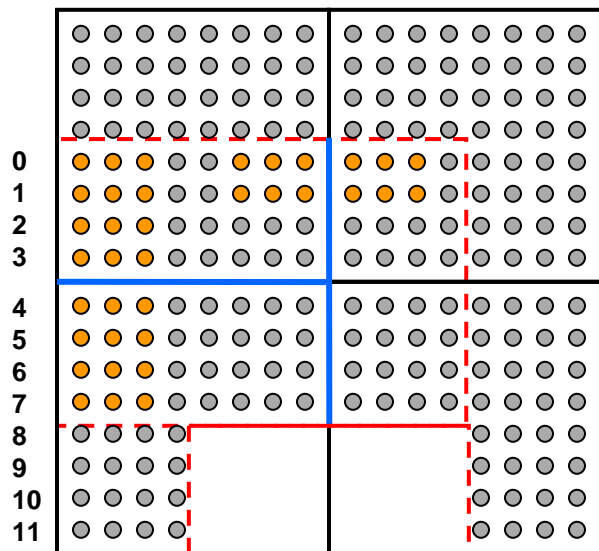
w/o parallel decision



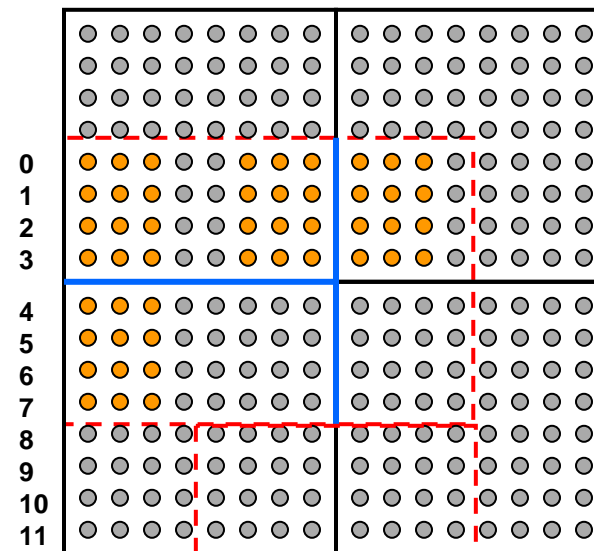
(a) initial buffer state



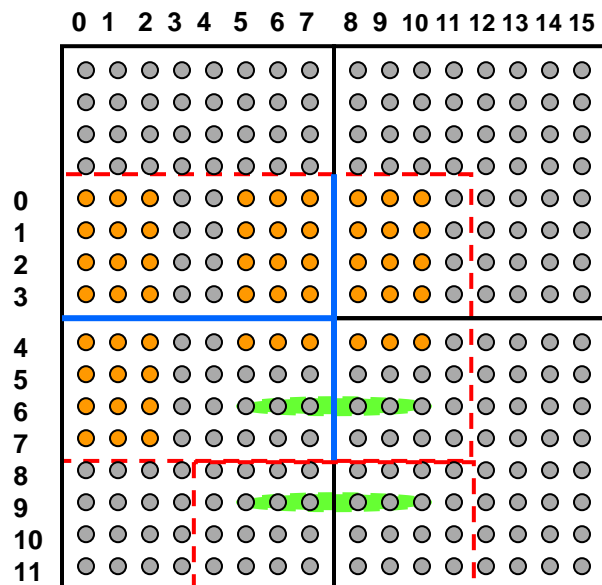
(b) Load line 0~3, 2 cycles



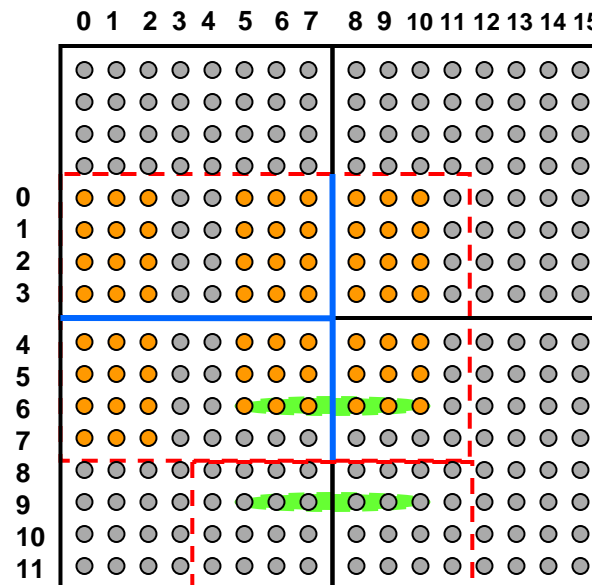
(c) Load line 4 ~ 7, process
line 0 & 1, 2 cycles



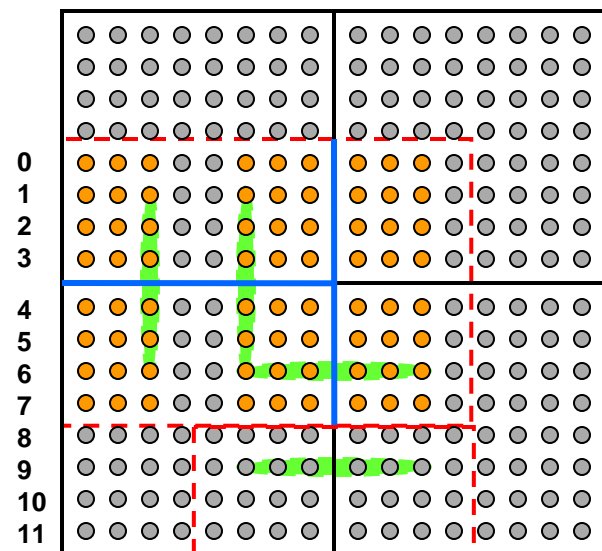
(d) Load line 8 ~ 11, process
line 2 & 3, 2 cycles



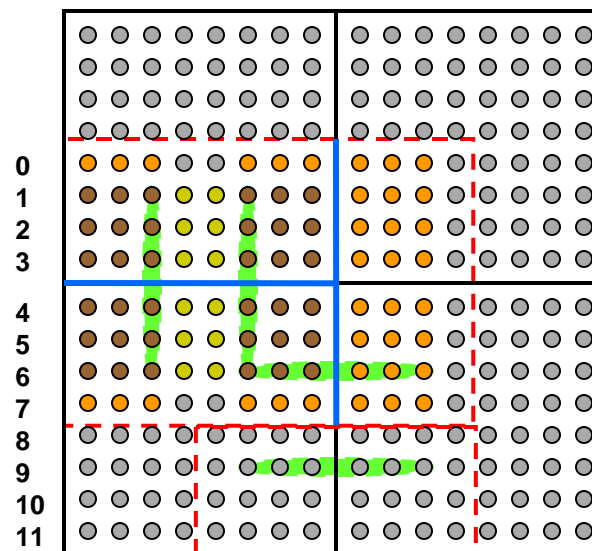
(e) Process line 4, vertical on/off decision, 1 cycle



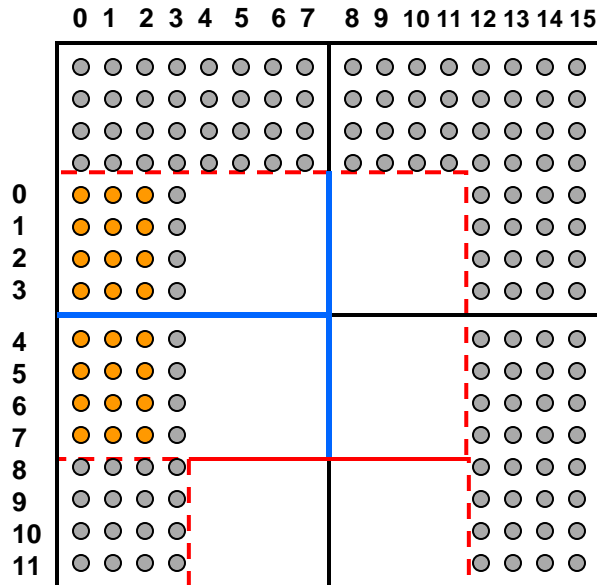
(f) Process line 5 ~ 6, 2 cycles



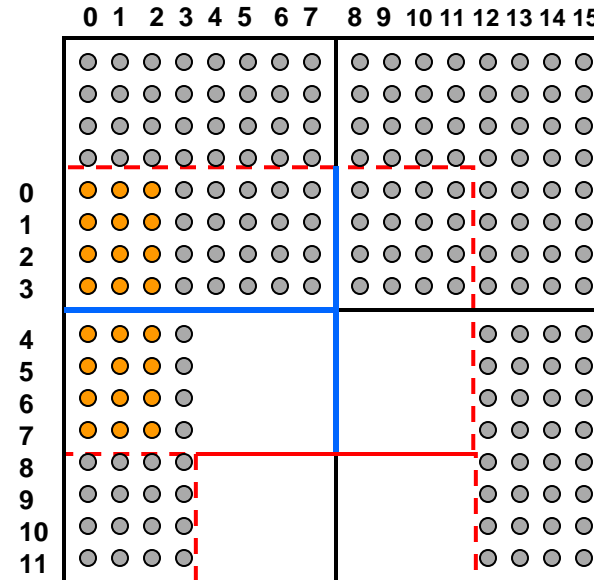
(g) Process line 7, horizontal on/off decision, 1 cycle



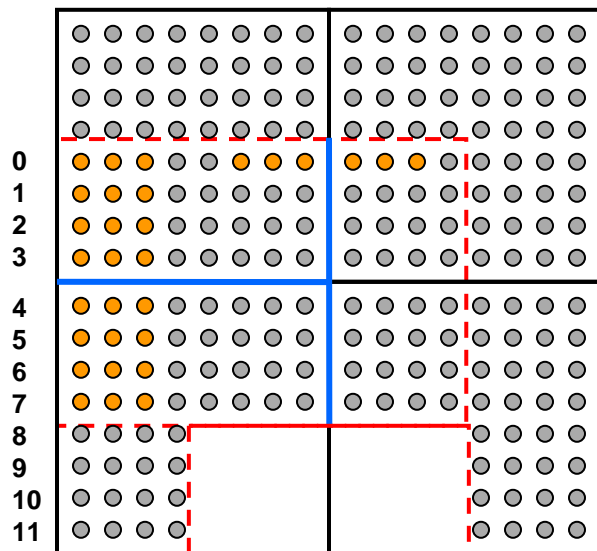
(h) Process column 0 ~ 7, 8 cycles



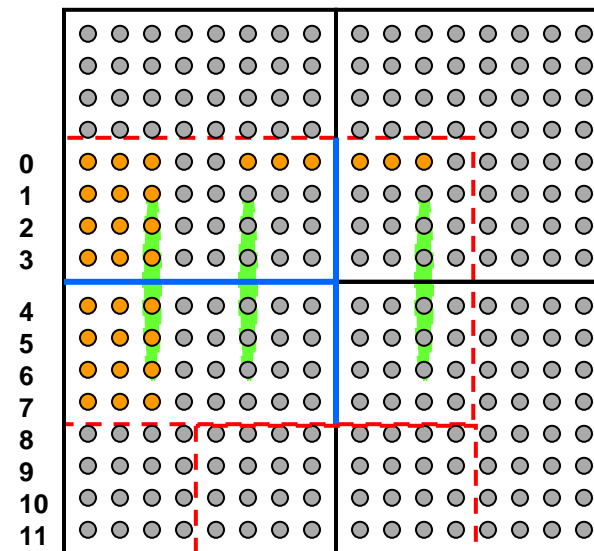
(a) initial buffer state



(b) Load line 0~3, 2 cycles

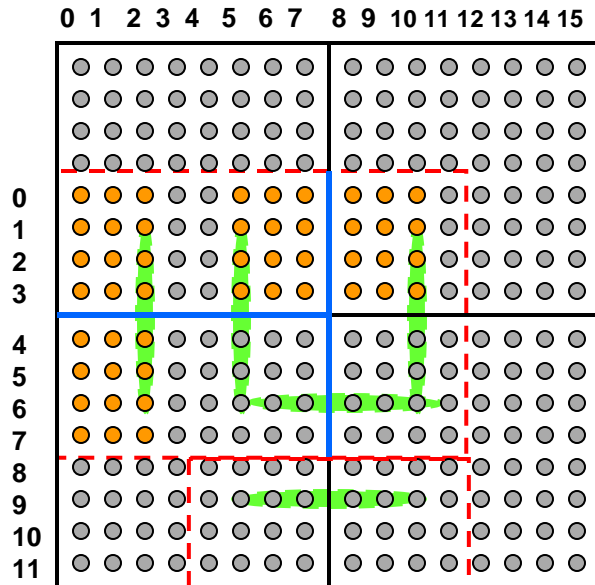


(c) Load line 4 ~ 7, process
line 0, 2 cycles

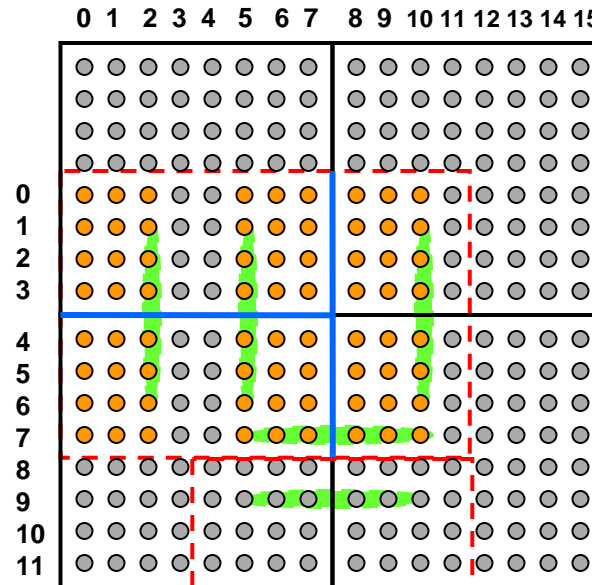


(d) Load line 8 ~ 11, horizontal on/off
decision, 2 cycles

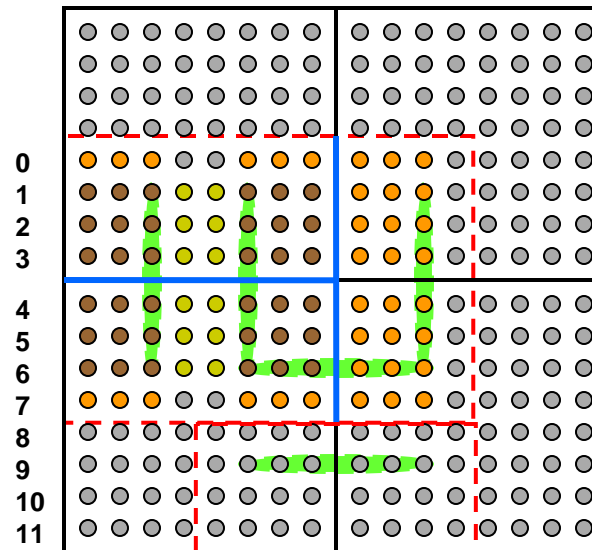
w/ parallel decision



(e) Process line 1, 2, 3, vertical edge on/off decision, 3 cycles



(f) Process line 4 ~ 7, 4 cycles

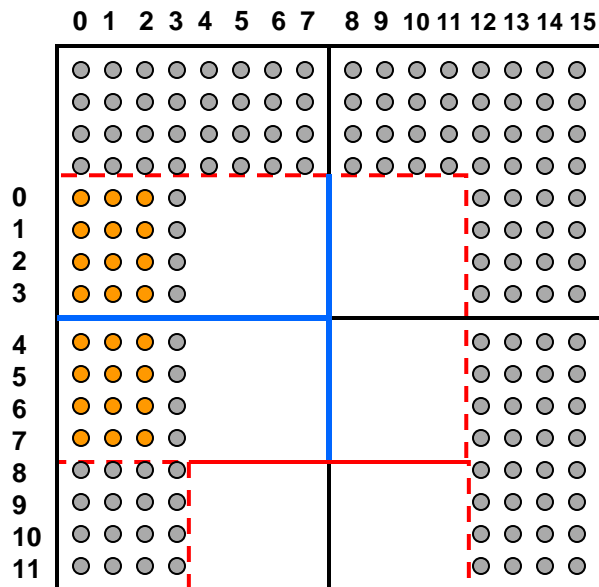


(g) Process column 0 ~ 7, 8 cycles

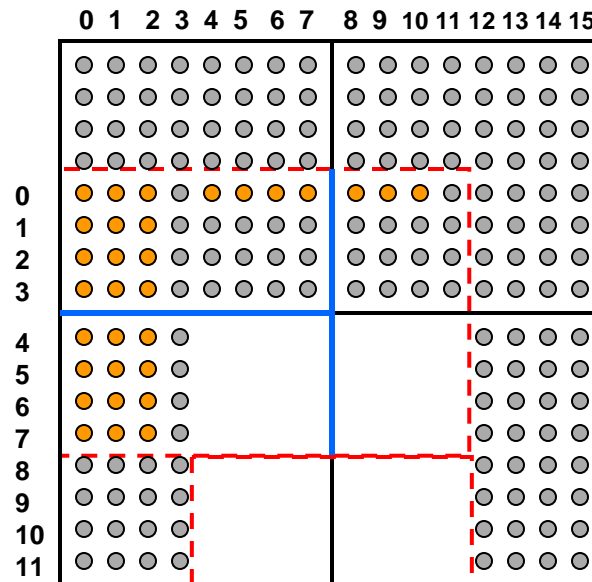
w/ parallel decision

Cycle estimate for line memory format

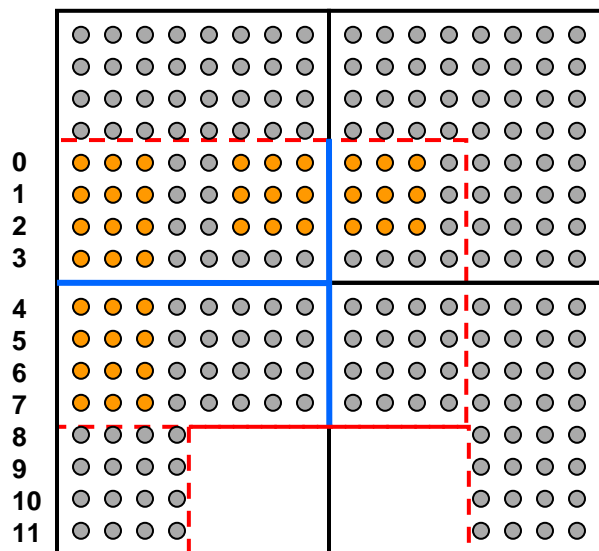
- Architecture assumptions
 - Single-cycle 8x2 (two lines) memory reads and writes
 - Single-cycle filtering for a line or column
 - Single-cycle filter on/off decision
 - Horizontal and vertical filtering shares a same logic
- Cycle count for 8x8 filtering area with same cost (cycle budget 50 cycles per 8x8)
 - w/o parallel decision 21 cycles
 - w/ parallel decision 24 cycles



(a) initial buffer state



(b) Load line 0~3, process line 0, 2 cycles

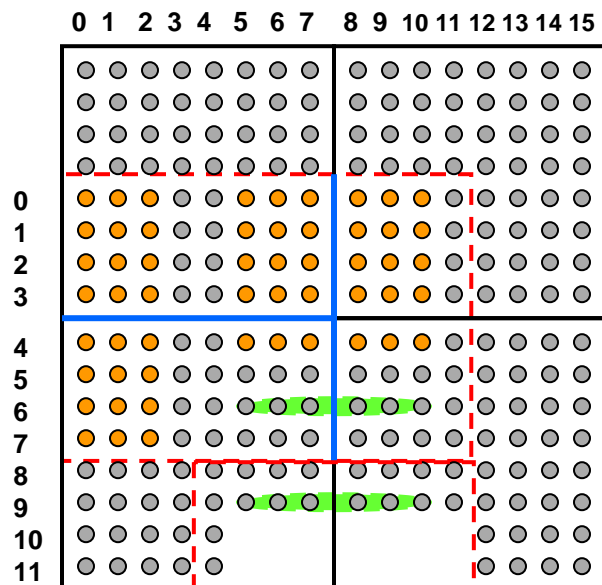


(c) Load line 4 ~ 7, process
line 1 & 2, 2 cycles

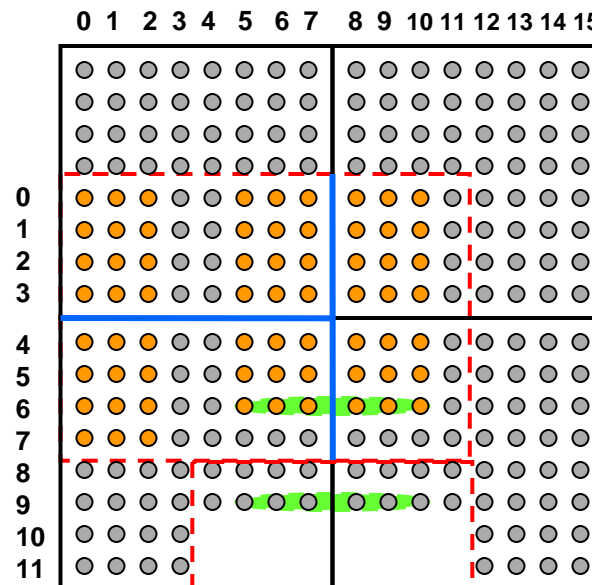


(d) Load line 8 ~ 9, process
line 3, 1 cycle

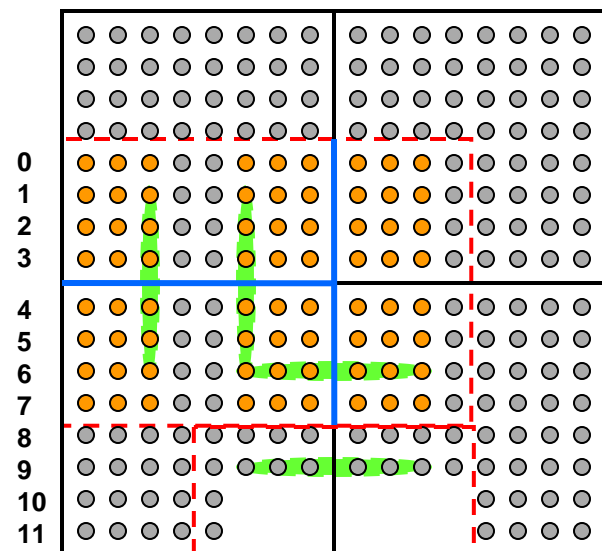
w/o parallel decision



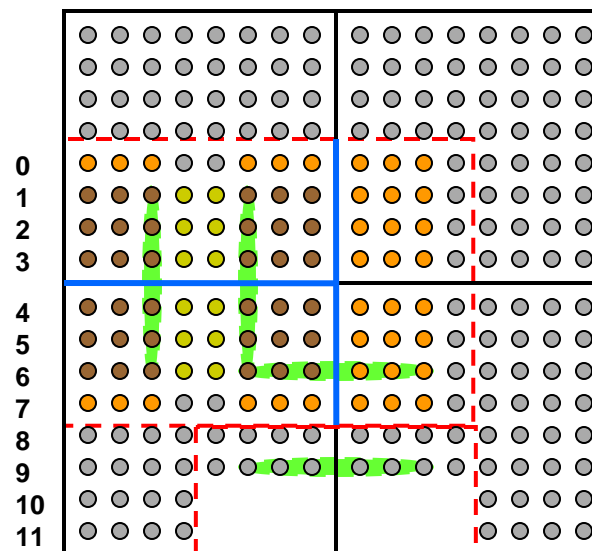
(e) Process line 4, vertical on/off decision, 1 cycle



(f) Process line 5 ~ 6, 2 cycles



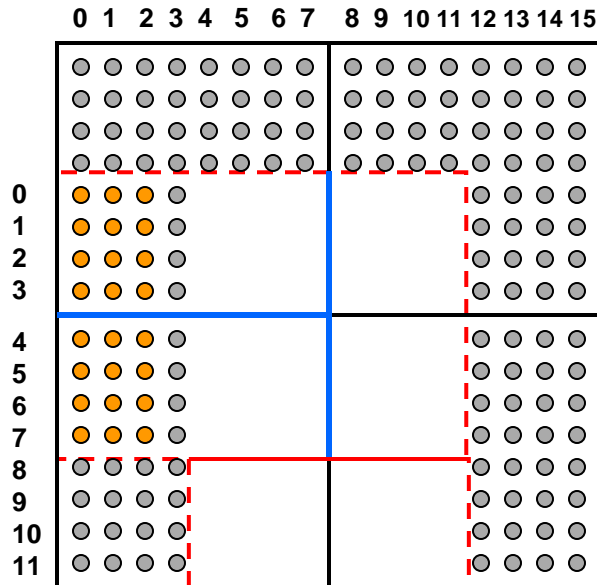
(g) Process line 7, horizontal on/off decision, 1 cycle



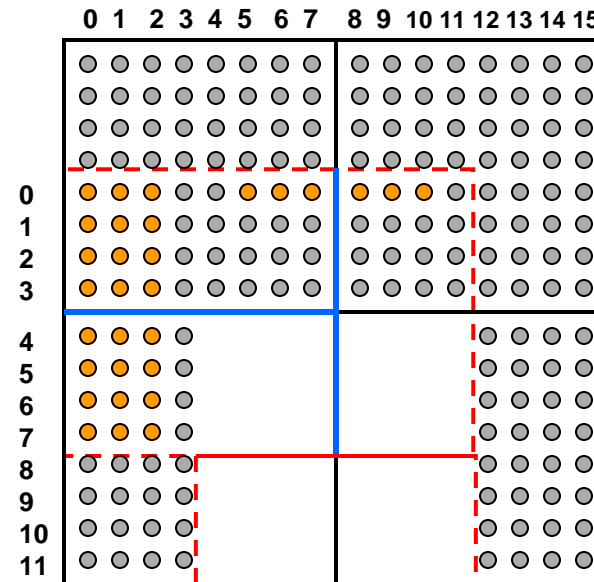
(h) Process column 0 ~ 7, 8 cycles

11/21/2011

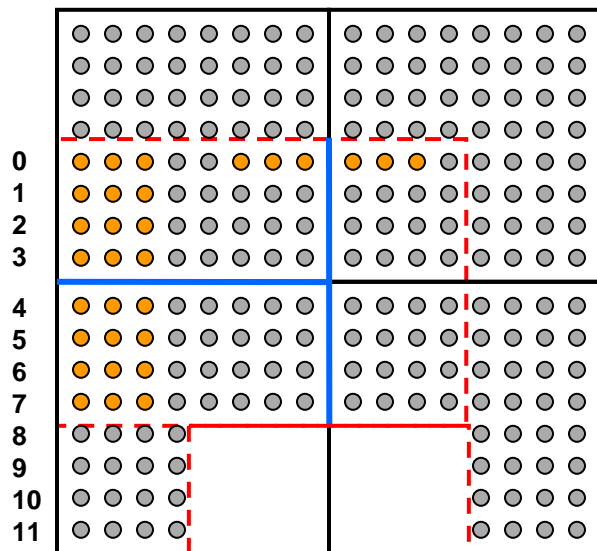
19



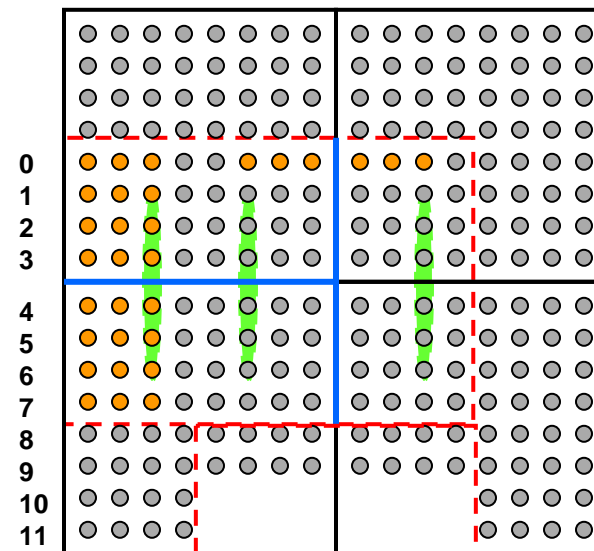
(a) initial buffer state



(b) Load line 0~3, process line 0, 2 cycles

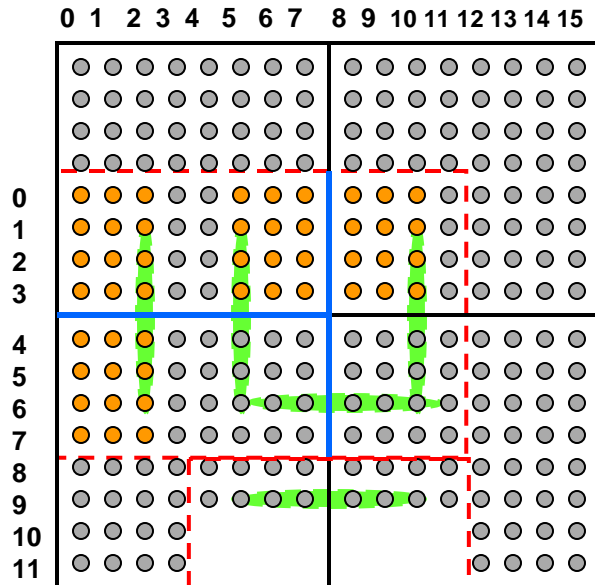


(c) Load line 4 ~ 7, process line 0, 2 cycles

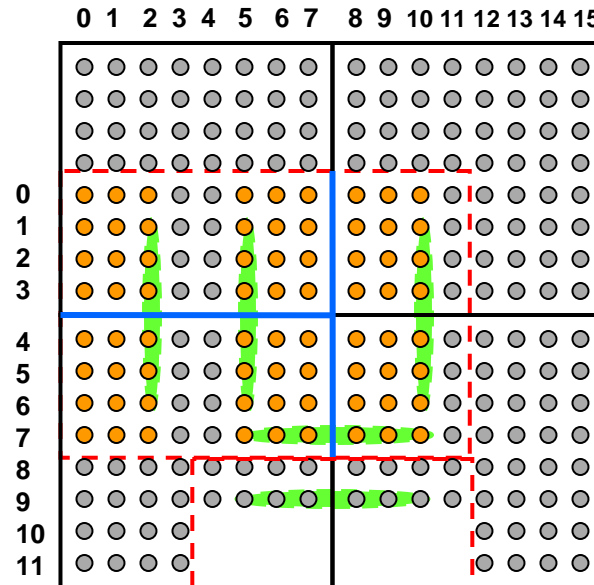


(d) Load line 8 ~ 9, horizontal on/off decision, 1 cycle

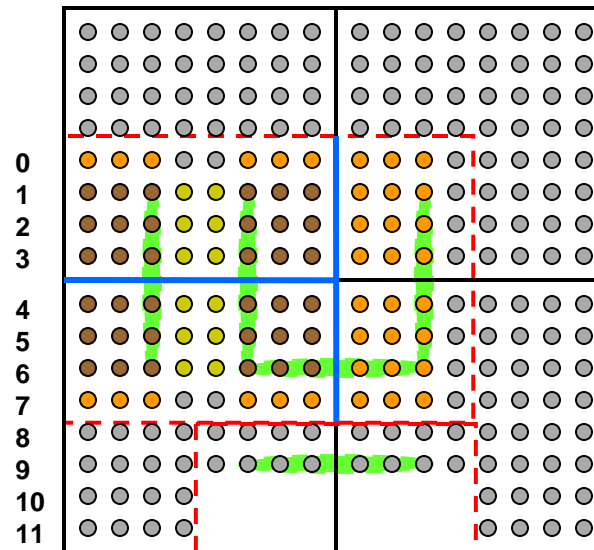
w/ parallel decision



(e) Process line 1, 2, 3, vertical on/off decision, 3 cycles



(f) Process line 4 ~ 7, 4 cycles



(g) Process column 0 ~ 7, 8 cycles

w/ parallel decision