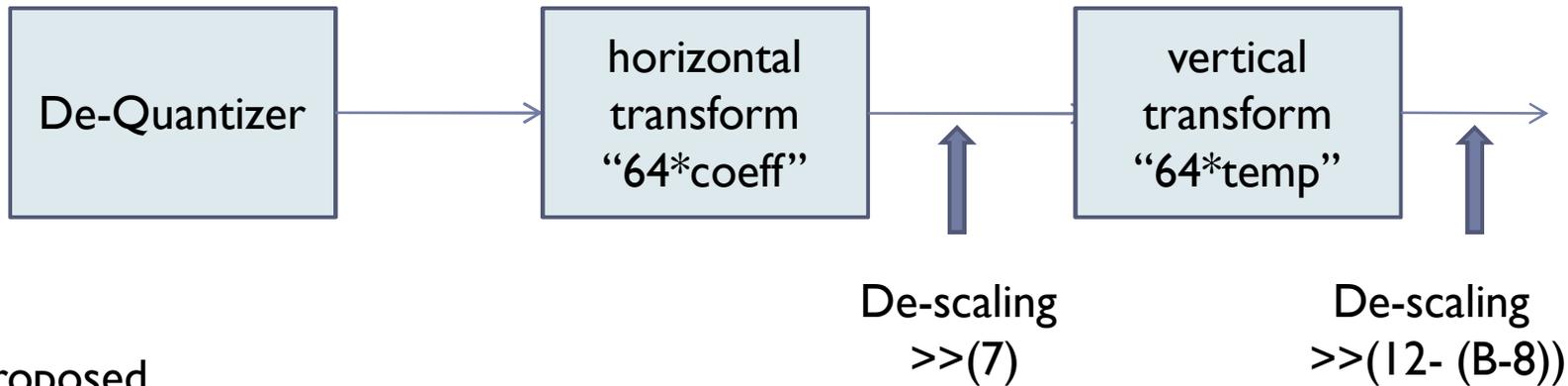


# **JCTVC-F251 CE10: Full-factorized core transform test by Samsung and FastVDO**

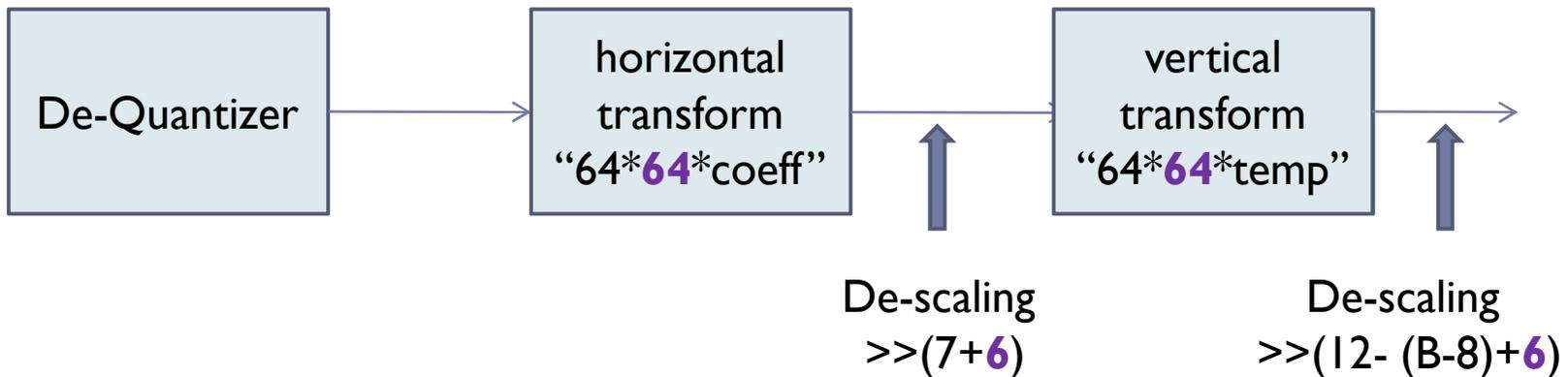
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Samsung Electronics Ltd  
Pankaj Topiwala, FastVDO

# Core transform framework

HM3.0



Proposed



...no change of buffers size after de-Quantizer, 1<sup>st</sup> (hor) and 2<sup>nd</sup> (vert) transforms...

# Transform matrix change

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HM3.0 transform matrix	Proposed transform matrix
{64, 64, 64, 64} {83, 36,-36,-83} {64,-64,-64, 64} {36,-83, 83,-36}	{ 4096, 4096, 4096, 4096}, { 5312, 2304,-2304,-5312}, { 4096,-4096,-4096, 4096}, { 2304,-5312, 5312,-2304}
{64, 64, 64, 64, 64, 64, 64, 64} {89, 75, 50, 18,-18,-50,-75,-89} {83, 36,-36,-83,-83,-36, 36, 83} {75,-18,-89,-50, 50, 89, 18,-75} {64,-64,-64, 64, 64,-64,-64, 64} {50,-89, 18, 75,-75,-18, 89,-50} {36,-83, 83,-36,-36, 83,-83, 36} {18,-50, 75,-89, 89,-75, 50,-18}	{ 4096, 4096, 4096, 4096, 4096, 4096, 4096, 4096}, { 5696, 4800, 3264, 1088,-1088,-3264,-4800,-5696}, { 5312, 2304,-2304,-5312,-5312,-2304, 2304, 5312}, { 4770,-1080,-5670,-3240, 3240, 5670, 1080,-4770}, { 4096,-4096,-4096, 4096, 4096,-4096,-4096, 4096}, { 3240,-5670, 1080, 4770,-4770,-1080, 5670,-3240}, { 2304,-5312, 5312,-2304,-2304, 5312,-5312, 2304}, { 1088,-3264, 4800,-5696, 5696,-4800, 3264,-1088},

... coefficients and basis vectors of the smaller transforms are a subset of coefficients and basis vectors of larger transforms...

# Three equivalent forms

- ▶ Flat quantization (==HM3.0) for all transform sizes
- ▶ 14 bit representation of transform coefficients
- ▶ Bit width of accumulators does not exceed 32 bit.
- ▶ Three equivalent forms

- ▶ Matrix multiplication form

- all multipliers don't exceed 16 bits
- number of mults in 32pt ID tr: **1024**

- ▶ Partial butterfly form

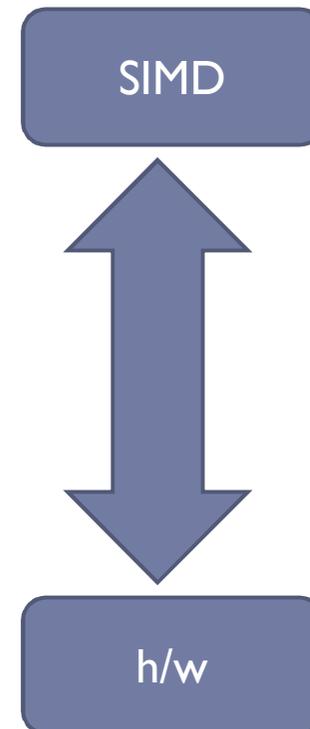
- all multipliers don't exceed 16 bits
- number of mults in 32pt ID tr: **344**

**HM3.0**

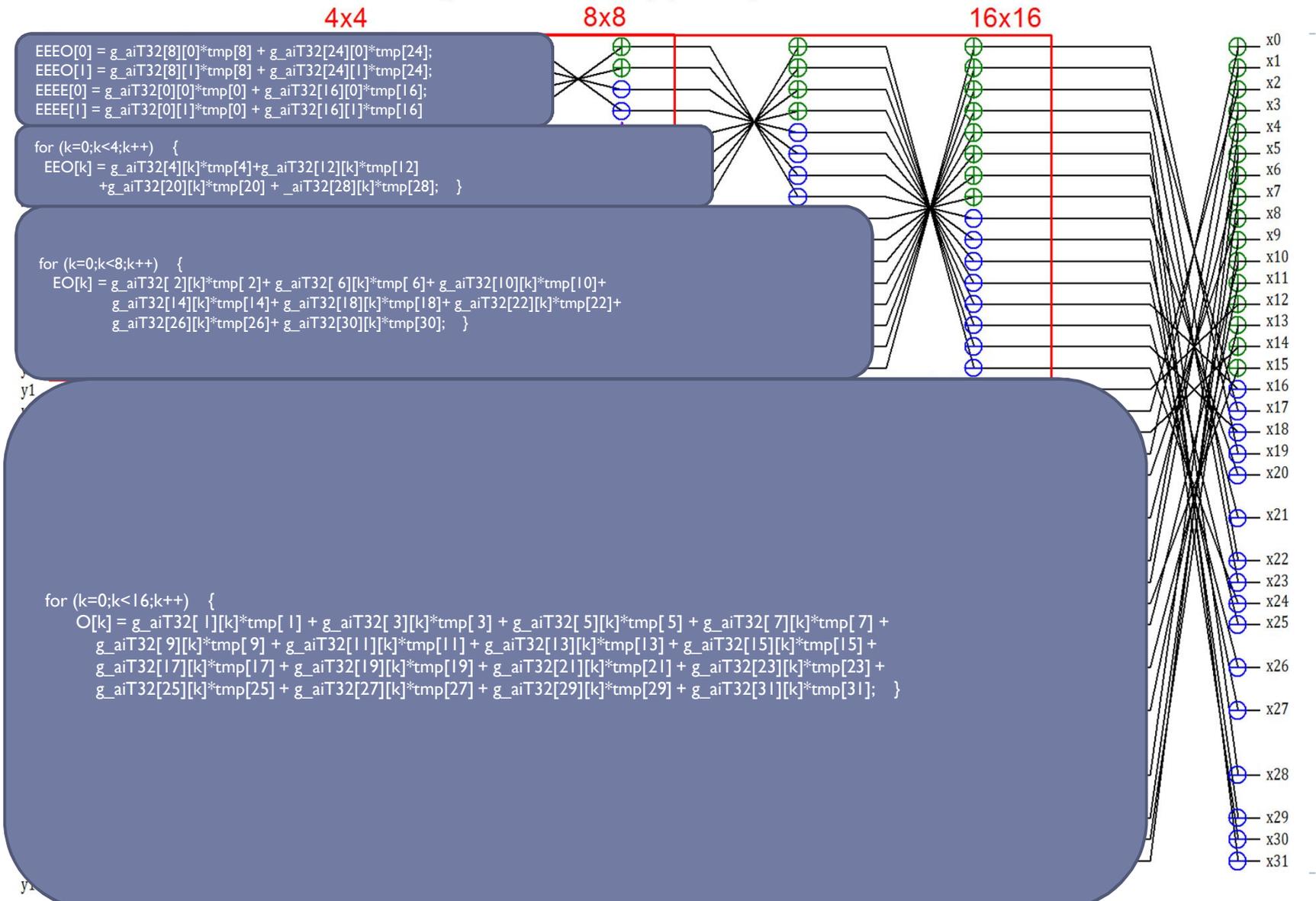
- ▶ Full-factorization form

- some multipliers exceed 16 bits
- number of mults in 32pt ID tr: **87**
- no de-scaling shift inside full butterfly

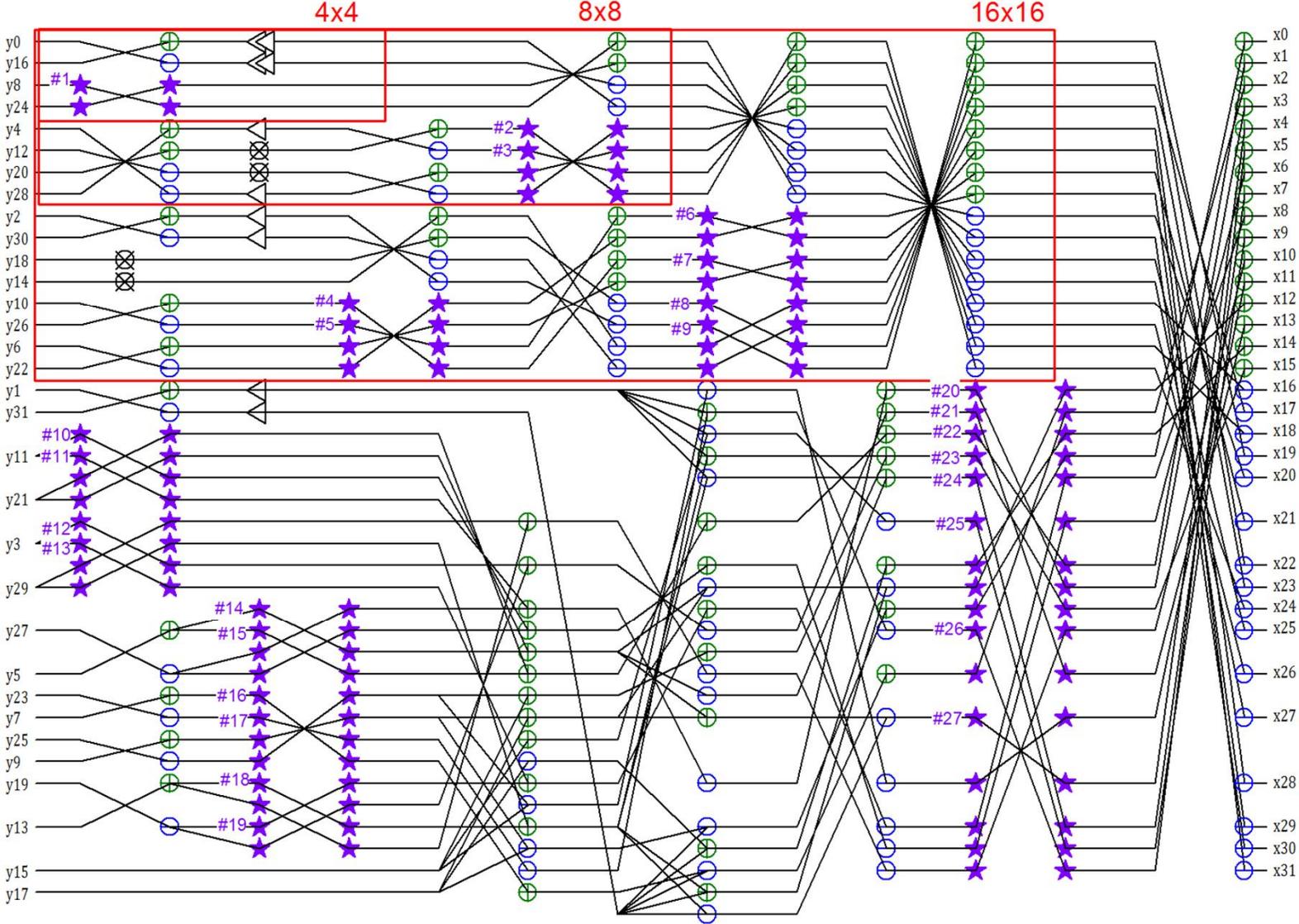
**Proposed**



# Partial butterfly flow graph == HM3.0



# Full-factorized flow graph



# Dynamic range analysis

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	IBDI ON				IBDI OFF			
	4×4	8×8	16×16	32×32	4×4	8×8	16×16	32×32
Output of inverse quantization	12	13	14	13	12	13	14	13
Input to the 1 <sup>st</sup> stage of inverse transform	16	16	16	14	16	16	16	14
Input to the 2 <sup>nd</sup> stage of inverse transform	15	16	16	15	15	16	16	15
Output of the 2 <sup>nd</sup> stage of inverse transform	11	12	12	12	9	10	10	10

The software framework provided by Cisco/TI was used as agreed in CEI0

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# H/w implementation analysis

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Frequency	Gate Count			
	HM3.0(partial butterfly)		FULL_FACTORIZATION	
150MHz	178,803	100%	135,480	76%
180MHz	205,971	100%	141,171	69%
200MHz	238,769	100%	147,153	62%

Frequency	Latency		Throughput Cycle
	HM3.0(partial butterfly)	FULL_FACTORIZATION	The same for both
150MHz	4	6	1
180MHz	4	5	1
200MHz	6	5	1

**Automatic RTL generation tool from C code, Catapult C of Mentor Graphics, is used to minimize the influence of level of optimization.**

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▶ JCTVC-F251 CE10: Full-factorized core transform test by Samsung and FastVDO

# Performance (normal QP)

	Intra			Intra LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.2	-0.1	-0.1	0.3	-0.1	-0.2
Class B	0.0	0.0	-0.1	0.1	-0.1	-0.1
Class C	0.0	0.0	0.0	0.0	0.0	-0.1
Class D	0.0	0.0	-0.1	0.0	0.0	0.0
Class E	0.0	-0.1	0.0	0.1	-0.1	0.0
<b>All</b>	<b>0.1</b>	<b>-0.1</b>	<b>-0.1</b>	<b>0.1</b>	<b>-0.1</b>	<b>-0.1</b>
Enc Time[%]	100%			97%		
Dec Time[%]	98%			96%		
	Random access			Random access LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.0	-0.2	-0.5	0.1	-0.2	-0.2
Class B	0.0	0.0	0.1	0.0	-0.1	-0.1
Class C	0.0	0.2	-0.2	0.0	-0.1	-0.1
Class D	0.0	-0.1	-0.2	0.0	-0.3	0.0
Class E						
<b>All</b>	<b>0.0</b>	<b>0.0</b>	<b>-0.2</b>	<b>0.0</b>	<b>-0.2</b>	<b>-0.1</b>
Enc Time[%]	99%			99%		
Dec Time[%]	99%			98%		
	Low delay			Low delay LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A						
Class B	0.0	0.1	-0.2	0.0	-0.1	-0.6
Class C	0.0	-0.1	-0.2	0.0	0.1	-0.2
Class D	-0.1	-0.1	0.2	0.0	0.0	0.0
Class E	0.0	-0.8	0.4	0.0	-0.2	-1.4
<b>All</b>	<b>0.0</b>	<b>-0.2</b>	<b>0.0</b>	<b>0.0</b>	<b>-0.1</b>	<b>-0.5</b>
Enc Time[%]	99%			99%		
Dec Time[%]	99%			97%		
<b>Avg 6 cases:</b>	<b>0.0</b>	<b>-0.1</b>	<b>-0.2</b>			

# Performance (low QP)

	Intra			Intra LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.8	0.3	0.3	1.0	0.7	0.7
Class B	0.3	0.0	0.0	0.3	0.1	0.0
Class C	0.1	0.0	0.0	0.7	0.3	0.3
Class D	0.1	0.0	0.0	0.8	0.4	0.4
Class E	0.1	0.0	0.0	0.2	-0.3	-0.2
<b>All</b>	<b>0.3</b>	<b>0.1</b>	<b>0.1</b>	<b>0.6</b>	<b>0.3</b>	<b>0.2</b>
Enc Time[%]	100%			98%		
Dec Time[%]	99%			101%		
	Random access			Random access LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.5	0.1	0.1	0.6	0.1	0.1
Class B	0.1	0.0	0.0	0.1	-0.1	-0.1
Class C	0.1	0.0	-0.1	0.2	0.1	0.0
Class D	0.0	-0.1	-0.1	0.2	0.0	0.1
Class E						
<b>All</b>	<b>0.2</b>	<b>0.0</b>	<b>0.0</b>	<b>0.3</b>	<b>0.0</b>	<b>0.0</b>
Enc Time[%]	100%			99%		
Dec Time[%]	99%			#VALUE!		
	Low delay			Low delay LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A						
Class B	0.1	0.0	0.0	0.2	0.0	-0.1
Class C	0.1	-0.1	-0.1	0.2	0.0	0.0
Class D	0.0	0.0	-0.1	0.1	-0.1	0.0
Class E	0.0	-0.1	-0.1	0.0	0.1	-0.1
<b>All</b>	<b>0.1</b>	<b>0.0</b>	<b>-0.1</b>	<b>0.1</b>	<b>0.0</b>	<b>0.0</b>
Enc Time[%]	100%			99%		
Dec Time[%]	99%			99%		
<b>Avg 6 cases:</b>	<b>0.3</b>	<b>0.0</b>	<b>0.0</b>			

# Performance (high QP)

	Intra			Intra LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	0.0	-0.2	1.5	0.1	-0.2	-0.2
Class B	0.0	-0.1	-0.4	0.0	-0.2	0.0
Class C	0.0	-0.5	0.2	0.0	-0.2	0.0
Class D	-0.1	2.2	0.3	0.1	-0.1	-0.1
Class E	0.0	-0.2	-0.1	0.0	0.1	-0.1
<b>All</b>	<b>0.0</b>	<b>0.3</b>	<b>0.3</b>	<b>0.0</b>	<b>-0.1</b>	<b>-0.1</b>
Enc Time[%]	100%			97%		
Dec Time[%]	95%			92%		
	Random access			Random access LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A	-0.1	-0.5	1.1	0.0	0.4	-2.3
Class B	0.1	-1.4	0.3	-0.2	0.5	0.1
Class C	-0.3	-1.3	1.5	-0.1	-2.2	0.3
Class D	-0.1	0.0	-0.3	-0.1	-1.0	0.0
Class E						
<b>All</b>	<b>-0.1</b>	<b>-0.9</b>	<b>0.6</b>	<b>-0.1</b>	<b>-0.5</b>	<b>-0.5</b>
Enc Time[%]	99%			99%		
Dec Time[%]	100%			98%		
	Low delay			Low delay LoCo		
	Y BD-rate	U BD-rate	V BD-rate	Y BD-rate	U BD-rate	V BD-rate
Class A						
Class B	0.0	0.6	-2.8	0.0	0.5	-1.4
Class C	-0.1	-0.4	0.0	-0.1	-1.1	-0.7
Class D	0.4	3.6	-0.5	-0.1	3.1	-0.7
Class E	0.1	-2.3	0.2	-0.4	1.6	0.7
<b>All</b>	<b>0.1</b>	<b>0.5</b>	<b>-1.0</b>	<b>-0.1</b>	<b>0.9</b>	<b>-0.7</b>
Enc Time[%]	100%			99%		
Dec Time[%]	99%			97%		
<b>Avg 6 cases:</b>	<b>0.0</b>	<b>0.1</b>	<b>-0.2</b>			

# Complexity/performance comparison of different proposals in CE10

		HM 3.0	QC(F352)	SEC(F251)	FastVDO(F363)
Complexity					
8-point	">>"	128	96	0	0
	"<<"	32	0	64	0
	Additions	448	416	464	448
	<b>Multiplications</b>	<b>352</b>	<b>192</b>	<b>176</b>	<b>384</b>
16-point	">>"	512	576	0	2880
	"<<"	64	0	192	512
	Additions	3200	2304	2592	4544
	<b>Multiplications</b>	<b>2752</b>	<b>1152</b>	<b>992</b>	<b>1216</b>
32-point	">>"	2048	2944	0	0
	"<<"	128	0	512	512
	Additions	23808	11904	14656	14656
	<b>Multiplications</b>	<b>21888</b>	<b>5888</b>	<b>5568</b>	<b>5568</b>
Performance					
Normal QP		0.0%/0.0%/0.0%	0.0%/0.1%/0.0%	0.0%/-0.1%/-0.2%	0.1%/0.0%/-0.1%
Low QP		0.0%/0.0%/0.0%	0.2%/0.3%/0.2%	0.3%/0.0%/0.0%	0.5%/0.2%/0.2%
High QP		0.0%/0.0%/0.0%	0.1%/-0.1%/0.2%	0.0%/0.0%/-0.2%	0.0%/-1.3%/-0.3%
AVG		0.0%/0.0%/0.0%	0.1%/0.1%/0.1%	0.1%/0.0%/-0.1%	0.2%/-0.4%/-0.1%



# Conclusion

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Based on test results:

0.0%/-0.1%/-0.2%

*(average performance across all 6 test cases in normal, low and high QP tests)*

we would like to recommend adoption for proposed core transform modification for HM4.0 and WD.

This will keep possibility of 2 equivalent implementations:

*matrix multiplication*

*partial butterfly*

available in HM3.0 and add one more equivalent implementation

*full-factorized form*

which will use 4 times smaller number of multiplications in 32 pt transform compare to default HM3.0 configuration (partial butterfly).

# SIMD implementation (F-710)

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		Total IFC	Called Count	Unit IFC
<b>C-Only Partial Butterfly</b>	E243	389312560	282520	1378
	F251	390219284	283178	1378
<b>SIMD Partial Butterfly</b>	E243	203979440	282520	722
	F251	204454516	283178	722
<b>SIMD Naive Matrix Multiplication</b>	E243	299471200	282520	1060
	F251	300168680	283178	1060
<b>SIMD Fast Matrix Multiplication</b>	E243	193243680	282520	684
	F251	193693752	283178	684

IFC == Instruction Fetch Cost

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