

Parallelized merge/skip mode for HEVC

JVTVC-F069

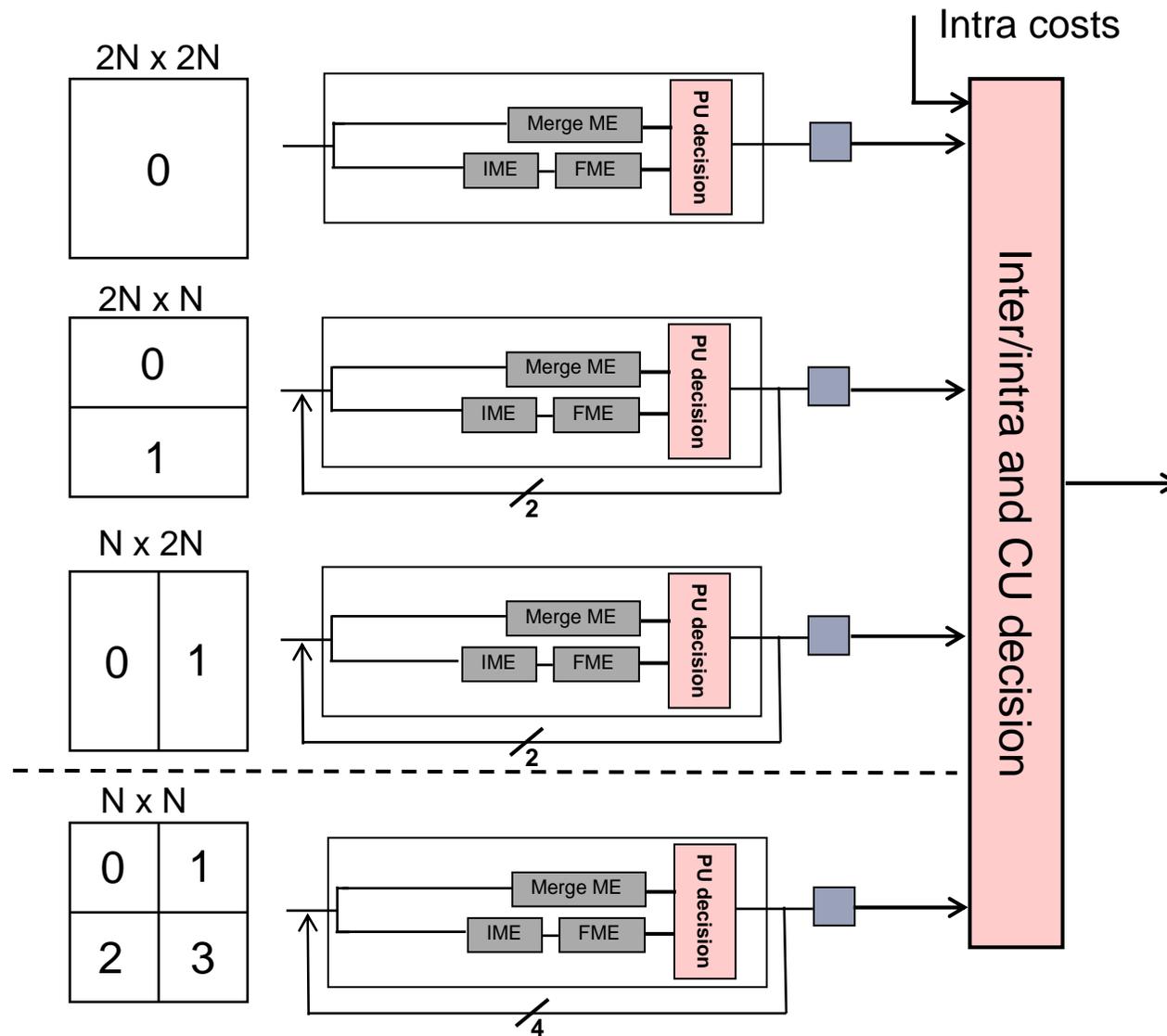
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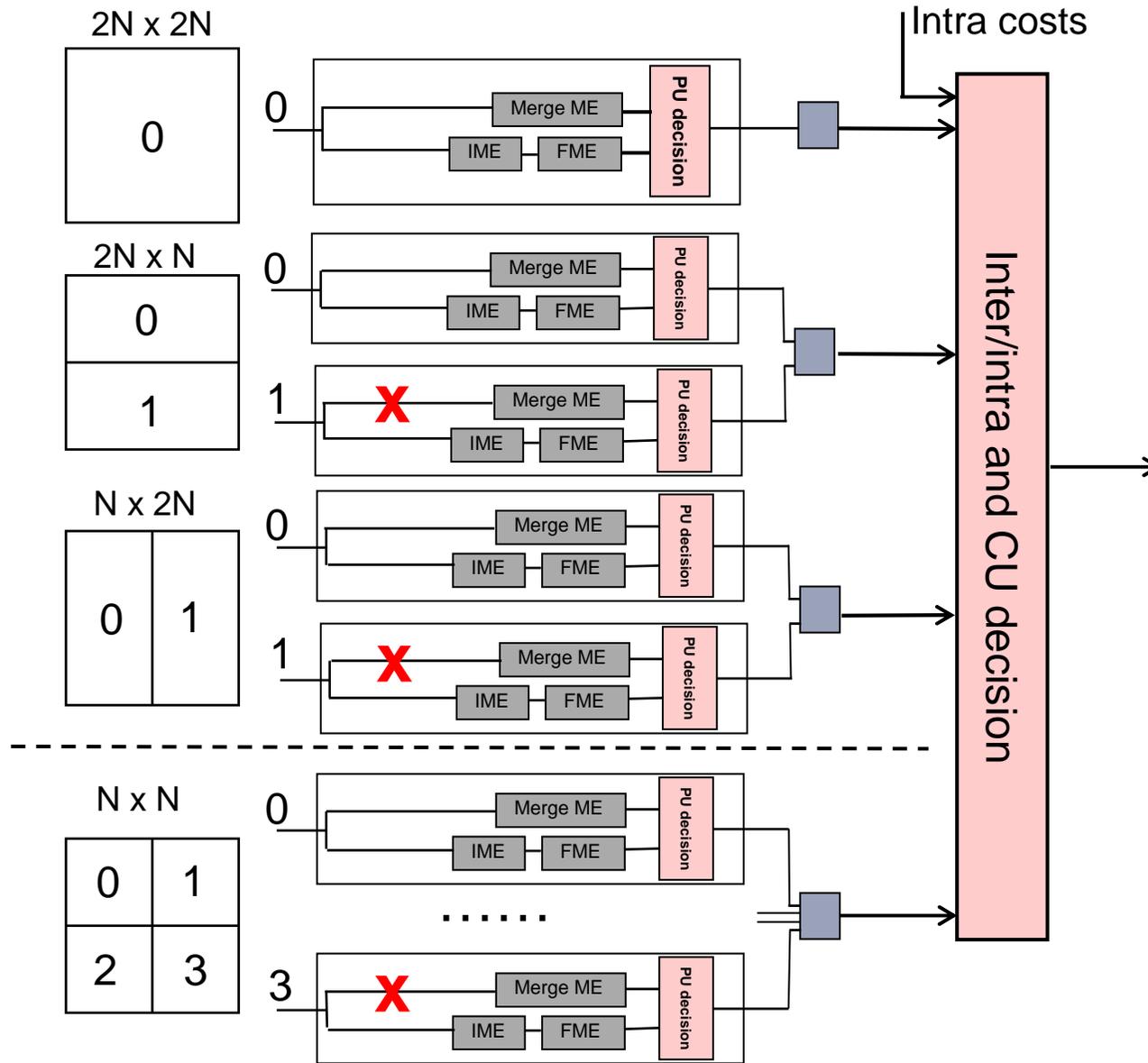
Motivation

- Current design of merge/skip mode in HM3.0 is highly sequential (down to 4x4) but has significant quality impact
- Parallel motion estimation (ME) at certain block level is required for practical encoder implementation due to throughput requirements and cost consideration
 - In the past typical parallel ME block level is 16x16 for e.g. AVC
 - Less a quality problem for AVC because skip mode operates at 16x16 level
- HEVC supports LCU size up to 64x64 and UHD
 - Higher parallel ME level may be required (e.g. 32x32)
 - More quality loss expected due to large block size
- Parallism of merge/skip mode should be improved

2Nx2N sequential ME engine architecture



2Nx2N parallel ME engine architecture



Quality loss at different parallel ME levels

Parallel ME level 2N x 2N (LCU = 64x64)	RA-HE (%)	RA-LC (%)	LB-HE (%)	LB-LC (%)
64 x 64	8.5	9.3	10.0	12.4
32 x 32	6.0	6.3	7.7	8.8
16 x 16	2.7	2.7	3.5	3.7
8 x 8	0.4	0.5	0.4	0.5

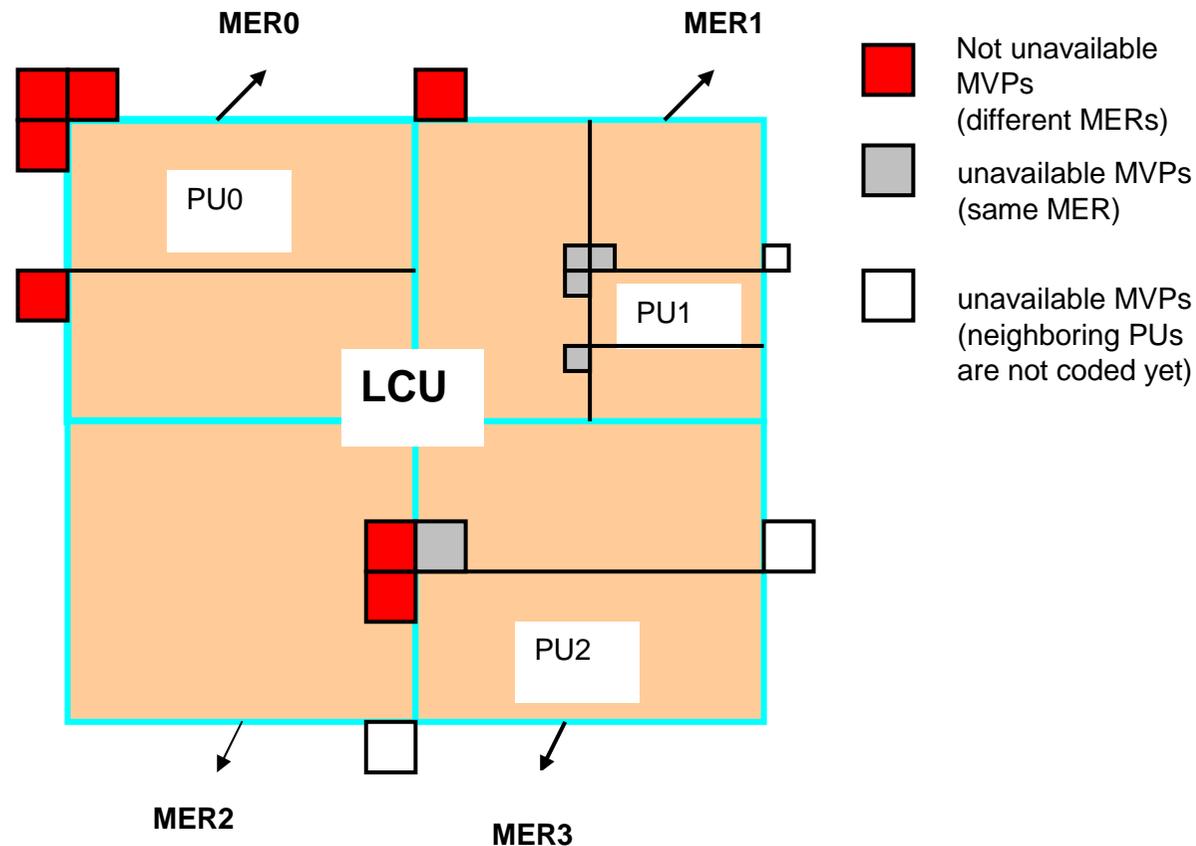
Only those PUs whose top-left corner sample is coincident with the top-left corner sample of the 2N x 2N block can test merge/skip mode in parallel to regular motion estimation.

Proposed algorithm

- Basic idea
 - Drop all the neighboring PUs whose motion data are still unavailable due to parallel ME from the merge/skip MVP list construction process, to enable parallel merge/skip search for all PU sizes
- Algorithm
 - Signal parallel merge level in PPS
 - Based on parallel merge level divide a LCU into non-overlapped ME regions (MER)
 - Only those PUs which belong to different MERs from the current PU are allowed to participate in the merge/skip MVP list construction process

Example

- A LCU is divided into four MERs based on parallel merge level
 - PU0: all neighboring PUs are available (same as HM3.0)
 - PU1: only temporal MVP is available
 - PU2: neighboring PUs are partially available



Signaling of parallel merge level

- Define a high-level element named **log2_parallel_merge_level_minus2** in PPS

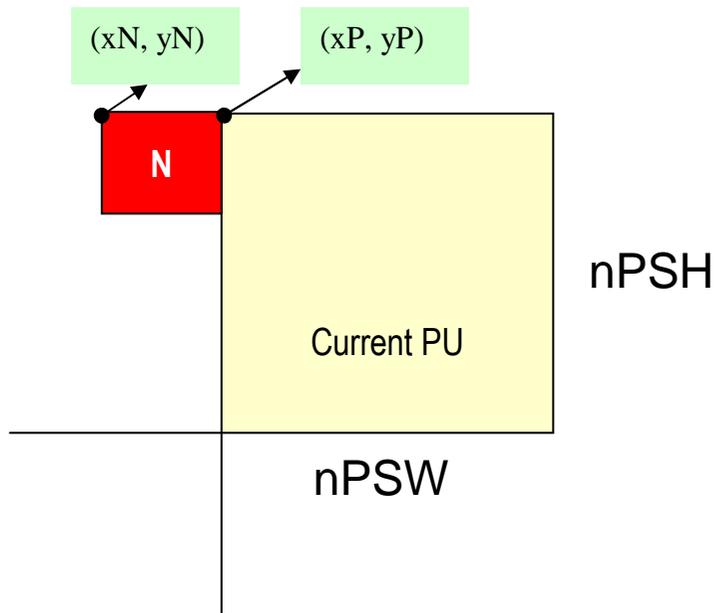
log2_parallel_merge_level_minus2	MER size	Remark
0	4x4	Sequential merge/skip mode for all PUs in a LCU because minimum PU size allowed by HEVC is 4x4 (same as HM3.0)
1	8x8	Parallel merge/skip mode search allowed for all PUs inside an 8x8 block
2	16x16	Parallel merge/skip mode search allowed for all PUs inside a 16x16 block
3	32x32	Parallel merge/skip mode search allowed for all PUs inside a 32x32 block
4	64x64	Parallel merge/skip mode search allowed for all PUs inside a 64x64 block

Decision on neighboring PU availability

- A neighboring PU is discarded from merge/skip MVP list construction process if

$$(x_P \gg (\log_2 \text{parallel_merge_level_minus}2+2)) == (x_N \gg (\log_2 \text{parallel_merge_level_minus}2+2))$$
 and

$$(y_P \gg (\log_2 \text{parallel_merge_level_minus}2+2)) == (y_N \gg (\log_2 \text{parallel_merge_level_minus}2+2))$$



(x_N, y_N)	Neighborhood relation
$(x_P - 4, y_P)$	Left
$(x_P, y_P - 4)$	Upper
$(x_P + nPSW, y_P - 4)$	Upper-right
$(x_P - 4, y_P + nPSH)$	Bottom-left

Experimental results

Loss from current HM3.0 design

Parallel ME level 2N x 2N (LCU = 64x64)	RA-HE (%)	RA-LC (%)	LB-HE (%)	LB-LC (%)
64 x 64	8.5	9.3	10.0	12.4
32 x 32	6.0	6.3	7.7	8.8
16 x 16	2.7	2.7	3.5	3.7
8 x 8	0.4	0.5	0.4	0.5

Loss from proposed algorithm

Parallel ME level 2N x 2N (LCU = 64x64)	RA-HE (%)	RA-LC (%)	LB-HE (%)	LB-LC (%)
64 x 64	3.7	3.6	4.1	4.4
32 x 32	2.1	2.1	2.2	2.4
16 x 16	0.8	0.7	0.5	0.7
8 x 8	0.1	0.0	-0.1	0.0

Relative gain at 32x32: 3.9% RA-HE, 4.2% RA-LC, 5.5% LB-HE, 6.4% LB-LC

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Summary

1. Merge/skip mode needs to be parallelized to facilitate high quality and high throughput HEVC encoder designs
2. The proposed algorithm introduces a high-level parameter to provide flexibility for high quality encoder designs at different parallel block levels
3. For typical parallel level at 32x32, the proposed algorithm achieved an average gain of **3.9% in RA-HE, 4.2% in RA-LC, 5.5% in LB-HE, 6.4% in LB-LC** when compared to the current design
4. Recommend to adopt this change in test model and set **log2_parallel_merge_level_minus2** to zero in common testing conditions

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