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| *Title:* | **CE6: Intra Prediction Improvements Summary Report** | | |
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# Abstract

This report provides the results of Core Experiment 6 (CE6) on Intra Prediction Improvements based on document JCTVC-E706.

# Introduction

Intra prediction improvement core experiments are divided into 5 categories

1. CE6.a: Block based Intra Prediction
2. CE6.b: Short Distance Intra Prediction (SDIP) Harmonization
3. CE6.c: Differential Coding of Intra Mode (DCIM)
4. CE6.d: Parallel Intra Coding
5. CE6.e: Intra Smoothing

# Experimental Conditions

## Software

CE6.a, CE6.c, CE6.d and CE6.e have been implemented into the HM3.0 software as recommended by the TM software group at the end of Geneva meeting. In addition, SDIP related subtests (CE6.b) have been integratedd into HM-SDIP software; and comparisons with HM-SDIP based anchors.

## Test Sequences, Bit Rates and Coding Conditions

In this CE, the recommended Test conditions of Intra-only configuration and Test sequences as defined in the document JCTVC-E700 and provided in the reference config files by the TM software group is used for all sub-CE tests.

## Evaluation of CE Results

Results of the CE are evaluated on the basis of BD-measures. No subjective evaluation to support the advantage of the proposed tools has been reported.

## Evaluation of Complexity

In general all the experiments are reporting the encode/decode run times. Detail description of each tool is expected in each sub-CE report.

# 

# Description of Tool Experiment

## CE6.a: Block Based Intra Prediction

### Bi-predictive Uni-Directional Intra (BUDI) Mode

JCTVC-E286 & JCTVC-D300 proposed Bi-predictive UDI Intra mode (BUDI) by using linear interpolation between two corresponding reference samples from main and side reference arrays, respectively. The purpose of this CE subset is to study the trade-off between coding performance and complexity. In addition, combination of BUDI with the adopted planar prediction will be considered.

The followings items will be investigated in this CE: (1) to study the performance of LUT-based and LUT-free implementations of BUDI; (2) To investigate on the different combinations of Intra mode signaling for BUDI, DC, and Planar modes.

### Test List

|  |  |  |  |
| --- | --- | --- | --- |
| **Core Experiments** | **Technology** | **Proponent(s)** | **Cross-checker(s)** |
| CE6.a.1 | LUT-based BUDI for HM and HM-SDIP |  | NEC, I2R |
| CE6.a.2 | LUT-free BUDI for HM and HM-SDIP |  | NEC, I2R |
| CE6.a.3 | LUT-based different combinations of Intra mode signaling for (DC,BUDI,Planar)=(2,6,9). |  | NEC, I2R |
| CE6.a.4 | LUT-free different combinations of Intra mode signaling for (DC,BUDI,Planar)=(2,6,9). |  | NEC, I2R |
| CE6.a.5 | LUT-based different combinations of Intra mode signaling for (DC,BUDI,Planar)=(9,6,2) |  | NEC, I2R |
| CE6.a.6 | LUT-free different combinations of Intra mode signaling for (DC,BUDI,Planar)=(9,6,2) |  | I2R |
| CE6.a.7 | LUT-based different combinations of Intra mode signaling for (DC,BUDI,Planar)=(2,9,6) |  | MS |
| CE6.a.8 | LUT-free different combinations of Intra mode signaling for (DC,BUDI,Planar)=(2,9,6) |  | MS |
| CE6.a.9 | LUT-based different combinations of Intra mode signaling for (DC,BUDI,Planar)=(6,9,2) |  | Qualcomm |
| CE6.a.10 | LUT-free different combinations of Intra mode signaling for (DC,BUDI,Planar)=(6,9,2) |  | Qualcomm |

### CE6.a Test results summary

The CE6.a.1 and CE6.a.2 are categorized as (1) the performance evaluation of LUT-based and LUT-free implementations of BUDI. The summary results for HM and HM-SDIP cases are shown in the following tables.

**Performance of LUT-based and LUT-free implementations of BUDI for HM**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Method  combination | AI - HE | | | | | AI – LC | | | | |
| BD-rate | | | Run time | | BD-rate | | | Run time | |
| Y | U | V | Enc | Dec | Y | U | V | Enc | Dec |
| CE6.a.1 LUT-based BUDI | -0.17 | 0.0 | 0.1 | 100 | 100 | -0.18 | -0.1 | 0.0 | 101 | 100 |
| CE6.a.2 LUT-free BUDI | -0.13 | 0.1 | 0.1 | 100 | 100 | -0.14 | 0.0 | 0.0 | 100 | 100 |

**Performance of LUT-based and LUT-free implementations of BUDI for HM-SDIP**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Method  combination | AI - HE | | | | | AI – LC | | | | |
| BD-rate | | | Run time | | BD-rate | | | Run time | |
| Y | U | V | Enc | Dec | Y | U | V | Enc | Dec |
| CE6.a.1 LUT-based BUDI | -0.19 | 0.0 | 0.0 | 99 | 100 | -0.20 | -0.1 | -0.1 | 100 | 100 |
| CE6.a.2 LUT-free BUDI | -0.14 | 0.1 | 0.1 | 100 | 99 | -0.15 | 0.0 | 0.0 | 99 | 99 |

The CE6.a.3-10 are categorized as (2) the performance evaluation of different combinations of Intra mode signaling for DC, BUDI, and Planar modes. The summary results for LUT-based and LUT-free HM on top of HM are shown in the following tables.

**Performance of different combinations of Intra mode signaling for DC, LUT-based BUDI, and Planar modes on top of HM**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Method  combination | AI - HE | | | | | AI – LC | | | | |
| BD-rate | | | Run time | | BD-rate | | | Run time | |
| Y | U | V | Enc | Dec | Y | U | V | Enc | Dec |
| CE6.a.3 (DC,BUDI,Planar)=(2,6,9) | -0.17 | 0.0 | 0.0 | 97% | 100% | -0.23 | 0.0 | 0.0 | 96% | 101% |
| CE6.a.5 (DC,BUDI,Planar)=(9,6,2) | -0.23 | 0.1 | 0.1 | 97% | 100% | -0.28 | 0.1 | 0.2 | 96% | 101% |
| CE6.a.7 (DC,BUDI,Planar)=(2,9,6) | -0.16 | 0.0 | 0.0 | 97% | 100% | -0.21 | 0.0 | 0.0 | 96% | 101% |
| CE6.a.9 (DC,BUDI,Planar)=(6,9,2) | -0.23 | 0.1 | 0.1 | 97% | 100% | -0.27 | 0.1 | 0.2 | 96% | 101% |

**Performance of different combinations of Intra mode signaling for DC, LUT-free BUDI, and Planar modes on top of HM**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Method  combination | AI - HE | | | | | AI – LC | | | | |
| BD-rate | | | Run time | | BD-rate | | | Run time | |
| Y | U | V | Enc | Dec | Y | U | V | Enc | Dec |
| CE6.a.4 (DC,BUDI,Planar)=(2,6,9) | -0.12 | 0.0 | 0.0 | 97% | 100% | -0.19 | 0.0 | 0.0 | 95% | 100% |
| CE6.a.6 (DC,BUDI,Planar)=(9,6,2) | -0.19 | 0.1 | 0.2 | 97% | 100% | -0.24 | 0.1 | 0.2 | 96% | 100% |
| CE6.a.8 (DC,BUDI,Planar)=(2,9,6) | -0.12 | 0.0 | 0.0 | 97% | 100% | -0.18 | 0.0 | 0.0 | 96% | 100% |
| CE6.a.10 (DC,BUDI,Planar)=(6,9,2) | -0.18 | 0.1 | 0.1 | 97% | 100% | -0.23 | 0.2 | 0.2 | 96% | 101% |

The following table shows summary results of combination of Intra mode signaling for DC=2, BUDI=6, and Planar=9 on top of HM-SDIP.

**Performance of combination of Intra mode signaling for DC=2, BUDI=6, and Planar=9 on top of HM-SDIP**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Method  combination | AI - HE | | | | | AI – LC | | | | |
| BD-rate | | | Run time | | BD-rate | | | Run time | |
| Y | U | V | Enc | Dec | Y | U | V | Enc | Dec |
| CE6.a.3 LUT-based BUDI | -0.15 | 0.0 | 0.0 | 97 | 99 | -0.20 | -0.1 | 0.0 | 97 | 100 |
| CE6.a.4 LUT-free BUDI | -0.10 | 0.0 | 0.0 | 97 | 100 | -0.15 | 0.0 | 0.1 | 96 | 100 |

## CE6.b: Short Distance Intra Prediction (SDIP) Harmonization (JCTVC-E278)

This CE subset is to complete and provide the harmonization solution that unifies the adopted SDIP features together with the remaining and existing HM tools from the conclusion of the 5th JCTVC meeting; test and confirm the SDIP performance in the harmonized software; revise and verify and confirm the potential WD text document matches the resulting new HM-SDIP software.

### Test List

|  |  |  |  |
| --- | --- | --- | --- |
| **Core Experiments** | **Technology** | **Proponent(s)** | **Cross-checker(s)** |
| CE6.b.1 | Test1 RQT Case1: Harmonization of SDIP and RQT Syntax | Tsinghua, USTC, HiSilicon, Microsoft, Huawei | NEC  Sony - match |
| CE.6.b.2 | Test1 RQT Case2: Harmonization of SDIP and two-depth RQT of 8x32/32x8 | Tsinghua, USTC, HiSilicon, Microsoft, Huawei | NEC  Sony - match |
| CE6.b.3 | Test2 DST Case1: Harmonization of SDIP and Mode-Dependent DCT/DST: SDIP=0, MDDT=0 | Huawei, HiSilicon | TI  Orange Lab - match |
| CE.6.b.4 | Test2 DST Case2: Harmonization of SDIP and Mode-Dependent DCT/DST: SDIP=1, MDDT=0 | Huawei, HiSilicon | NEC - match  BBC - match |
| CE6.b.5 | Test2 DST Case3: Harmonization of SDIP and Mode-Dependent DCT/DST: SDIP=1, (MDDT=1 & SDIP\_MDDT=1) | Huawei, HiSilicon | TI ... testing |
| CE.6.b.6 | Test3 MDCS: Harmonization of SDIP and MDCS: SDIP=1, (MDCS=1&SDIP\_MDCS=0) | Microsoft | NEC - match  Sony - match  INRIA - match |
| CE6.b.7 | Test4 LM: Harmonization of LM mode and the chroma prediction in SDIP: SDIP=1 | LGE, Microsoft | Sharp - match (LGE) |
| CE.6.b.8 | Test5 MDIS Case1: Harmonization of SDIP and MDIS: SDIP=0, MDIS=0 | Santa Clara University, HiSilicon | Qualcomm - match |
| CE6.b.9 | Test5 MDIS Case2: Harmonization of SDIP and MDIS: SDIP=1, MDIS=0 | Santa Clara University, HiSilicon | Qualcomm - match |
| CE.6.b.10 | Test5 MDIS Case3: Harmonization of SDIP and MDIS: SDIP=1, (MDIS=1&SDIP\_MDIS=1) | Santa Clara University, HiSilicon | NEC - match |
| CE.6.b.10.1 | Test5 MDIS Qualcomm Test Case | Qualcomm | Ghent University - match |
| CE6.b.11 | Test6 Planar Case1: Harmonization of SDIP and PLANAR: SDIP=0, PLANAR=0 | HiSilicon, Tsinghua | Canon - match |
| CE.6.b.12 | Test6 Planar Case2: Harmonization of SDIP and PLANAR: SDIP=1, PLANAR=0 | HiSilicon, Tsinghua | Canon - match |
| CE6.b.13 | Test6 Planar Case3: Harmonization of SDIP and PLANAR: SDIP=1, (PLANAR=1&SDIP\_PLANAR=1) | HiSilicon, Tsinghua | Canon - match |

|  |  |  |  |
| --- | --- | --- | --- |
| CE.6.b.14 | Test7 LF Case1 : Harmonization of SDIP and deblocking filter: SDIP=0, deblocking filter=0 | Tsinghua, HiSilicon | Qualcomm ... testing |
| CE6.b.15 | Test7 LF Case2 : Harmonization of SDIP and deblocking filter: SDIP=1, deblocking filter=0 | Tsinghua, HiSilicon | Qualcomm - match  NEC - match |
| CE.6.b.16 | Test7 LF Case3 : Harmonization of SDIP and deblocking filter: SDIP=1, (deblocking filter=1&SDIP\_deblocking filter=1) | Tsinghua, HiSilicon | NEC - match |
| CE6.b.16.1 | Harmonization of SDIP and deblocking filter | Qualcomm | Mediatek .... testing |
| CE6.b.17 | Test8 DC prediction filtering Case1: Harmonization of SDIP and DC prediction filtering: SDIP=0, DC prediction filter = 0 | Qualcomm | HiSilicon .... testing |
| CE.6.b.18 | Test8 DC prediction filtering Case2: Harmonization of SDIP and DC prediction filtering: SDIP=1, DC prediction filter = 0 | Qualcomm | HiSilicon .... testing |

### CE6.b.1 Test results summary

#### Test1: Harmonization of SDIP and RQT

Case1:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LC | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | -0.02 | 0.11 | 0.21 | -0.17 | -0.66 | -0.50 |
| Class B | -0.02 | 0.20 | 0.23 | -0.22 | -0.55 | -0.54 |
| Class C | -0.03 | 0.22 | 0.24 | -0.26 | -0.49 | -0.47 |
| Class D | -0.03 | 0.23 | 0.18 | -0.23 | -0.36 | -0.33 |
| Class E | -0.03 | 0.25 | 0.25 | -0.31 | -1.09 | -1.10 |
| **All** | **-0.03** | **0.20** | **0.22** | **-0.24** | **-0.61** | **-0.56** |
| Enc Time[%] | 100% | | | 102% | | |
| Dec Time[%] | 101% | | | 102% | | |

Case 2:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LC | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | -0.03 | -0.02 | 0.12 | -0.16 | -0.62 | -0.46 |
| Class B | -0.21 | -0.22 | -0.18 | -0.57 | -0.66 | -0.63 |
| Class C | -0.06 | 0.12 | 0.12 | -0.32 | -0.51 | -0.50 |
| Class D | -0.09 | 0.14 | 0.12 | -0.31 | -0.37 | -0.34 |
| Class E | -0.47 | -0.46 | -0.42 | -0.86 | -1.33 | -1.14 |
| **All** | **-0.16** | **-0.08** | **-0.04** | **-0.43** | **-0.66** | **-0.59** |
| Enc Time[%] | 101% | | | 103% | | |
| Dec Time[%] | 100% | | | 101% | | |

#### Test2: Harmonization of SDIP and Mode-Dependent DCT/DST

Case1 (positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | 0.67 | 0.19 | 0.19 | 0.71 | 0.36 | 0.44 |
| Class B | 0.66 | 0.33 | 0.28 | 0.85 | 0.54 | 0.47 |
| Class C | 0.81 | 0.58 | 0.60 | 1.32 | 0.77 | 0.67 |
| Class D | 0.88 | 0.76 | 0.77 | 1.37 | 0.78 | 0.74 |
| Class E | 0.99 | 0.58 | 0.80 | 1.33 | 0.50 | 0.67 |
| **Overall** | **0.79** | **0.47** | **0.50** | **1.09** | **0.59** | **0.59** |
| Enc Time[%] | 99% | | | 99% | | |
| Dec Time[%] | 100% | | | 99% | | |

Case2 (positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | 0.56 | 0.06 | 0.05 | 0.49 | 0.26 | 0.28 |
| Class B | 0.52 | 0.13 | 0.02 | 0.54 | 0.30 | 0.22 |
| Class C | 0.55 | 0.29 | 0.20 | 0.80 | 0.38 | 0.30 |
| Class D | 0.58 | 0.36 | 0.33 | 0.86 | 0.38 | 0.39 |
| Class E | 0.78 | -0.02 | 0.21 | 0.85 | 0.01 | 0.18 |
| **Overall** | **0.59** | **0.17** | **0.15** | **0.69** | **0.28** | **0.28** |
| Enc Time[%] | 100% | | | 99% | | |
| Dec Time[%] | 100% | | | 99% | | |

Case3:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | -0.02 | -0.19 | -0.19 | -0.09 | -0.14 | -0.20 |
| Class B | -0.02 | -0.12 | -0.17 | -0.06 | -0.11 | -0.16 |
| Class C | -0.02 | -0.20 | -0.19 | -0.08 | -0.17 | -0.20 |
| Class D | -0.02 | -0.13 | -0.16 | -0.03 | -0.11 | -0.13 |
| Class E | -0.09 | -0.42 | -0.51 | -0.22 | -0.60 | -0.56 |
| **Overall** | **-0.03** | **-0.20** | **-0.23** | **-0.09** | **-0.20** | **-0.23** |
| Enc Time[%] | 99% | | | 100% | | |
| Dec Time[%] | 100% | | | 99% | | |

#### Test3: Harmonization of SDIP and MDCS (positive means gain here)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LoCo | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | 0.01 | 0.06 | 0.05 | 0.03 | 0.08 | 0.10 |
| Class B | 0.05 | 0.05 | 0.03 | 0.06 | 0.10 | 0.13 |
| Class C | 0.16 | 0.16 | 0.17 | 0.15 | 0.18 | 0.20 |
| Class D | 0.18 | 0.19 | 0.16 | 0.11 | 0.09 | 0.11 |
| Class E | 0.02 | -0.05 | -0.04 | 0.02 | 0.10 | 0.05 |
| **All** | **0.08** | **0.09** | **0.08** | **0.08** | **0.11** | **0.12** |
| Enc Time[%] | 100% | | | 100% | | |
| Dec Time[%] | 100% | | | 100% | | |

#### Test4: Harmonization of LM mode and the chroma prediction in SDIP

1.LGE test case:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | |  | All Intra LC | | |
|  | Y | U | V | Y | U | V |
| Class A | -0.03 | -0.05 | -0.05 | 0.00 | -0.49 | -0.07 |
| Class B | 0.03 | -0.15 | -0.19 | 0.01 | -0.21 | -0.07 |
| Class C | -0.07 | -0.34 | -0.22 | -0.07 | -0.34 | -0.30 |
| Class D | -0.06 | -0.30 | -0.26 | -0.06 | -0.27 | -0.18 |
| Class E | 0.06 | -0.42 | -0.46 | 0.02 | -0.08 | -0.18 |
| **Overall** | **-0.02** | **-0.24** | **-0.22** | **-0.02** | **-0.29** | **-0.15** |
| Enc Time[%] | 100% |  |  | 99% |  |  |
| Dec Time[%] | 100% |  |  | 100% |  |  |

2.Microsoft test case ( positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LoCo | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | 0.01 | 0.34 | 0.38 | 0.03 | 1.02 | 0.54 |
| Class B | 0.03 | 0.52 | 0.52 | 0.07 | 0.76 | 0.68 |
| Class C | 0.13 | 1.03 | 0.99 | 0.21 | 1.27 | 1.28 |
| Class D | 0.09 | 0.64 | 0.54 | 0.13 | 0.85 | 0.69 |
| Class E | 0.02 | 0.50 | 0.49 | 0.06 | 0.93 | 1.07 |
| **All** | **0.06** | **0.61** | **0.59** | **0.10** | **0.96** | **0.83** |
| Enc Time[%] | 100% | | | 101% | | |
| Dec Time[%] | 100% | | | 100% | | |

#### Test5: Harmonization of SDIP and MDIS

**1. HiSilicon & Santa Clara University test cases**

Case1(positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | 0.40 | 0.38 | 0.70 | 0.65 | 0.45 | 0.75 |
| Class B | 0.19 | 0.27 | 0.25 | 0.33 | 0.19 | 0.18 |
| Class C | -0.13 | -0.04 | 0.00 | -0.34 | -0.13 | -0.18 |
| Class D | 0.06 | 0.10 | 0.16 | 0.10 | 0.10 | 0.08 |
| Class E | 0.31 | 0.51 | 0.52 | 0.59 | 0.46 | 0.43 |
| **Overall** | **0.16** | **0.23** | **0.31** | **0.25** | **0.20** | **0.24** |
| Enc Time[%] | 99% | | | 98% | | |
| Dec Time[%] | 99% | | | 98% | | |

Case2 (positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | 0.37 | 0.22 | 0.51 | 0.53 | 0.25 | 0.47 |
| Class B | 0.20 | 0.27 | 0.23 | 0.29 | 0.21 | 0.25 |
| Class C | -0.04 | 0.09 | 0.11 | -0.06 | 0.10 | 0.04 |
| Class D | 0.06 | 0.19 | 0.12 | 0.12 | 0.10 | 0.08 |
| Class E | 0.36 | 0.42 | 0.30 | 0.59 | 0.39 | 0.38 |
| **Overall** | **0.18** | **0.23** | **0.25** | **0.28** | **0.20** | **0.24** |
| Enc Time[%] | 99% | | | 97% | | |
| Dec Time[%] | 99% | | | 97% | | |

Case3:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | -0.04 | -0.19 | -0.14 | -0.12 | -0.04 | -0.12 |
| Class B | 0.00 | 0.04 | 0.04 | -0.02 | 0.07 | 0.09 |
| Class C | 0.04 | 0.06 | 0.04 | 0.08 | 0.02 | 0.04 |
| Class D | -0.01 | 0.03 | -0.05 | -0.01 | 0.01 | -0.01 |
| Class E | 0.03 | -0.07 | 0.00 | 0.02 | 0.13 | 0.10 |
| **Overall** | **0.00** | **-0.02** | **-0.02** | **-0.01** | **0.03** | **0.02** |
| Enc Time[%] | 100% | | | 100% | | |
| Dec Time[%] | 100% | | | 100% | | |

**2.Qualcomm test case**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | -0.1 | -0.2 | -0.1 | -0.1 | -0.1 | -0.1 |
| Class B | -0.1 | -0.2 | -0.2 | -0.1 | -0.1 | -0.1 |
| Class C | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 | -0.1 |
| Class D | 0.0 | 0.0 | -0.1 | 0.0 | 0.0 | 0.0 |
| Class E | -0.1 | -0.3 | -0.2 | 0.0 | -0.2 | -0.2 |
| **Overall** | **-0.1** | **-0.2** | **-0.1** | **-0.1** | **-0.1** | **-0.1** |
| Enc Time[%] | 100% | | | 101% | | |
| Dec Time[%] | 99% | | | 99% | | |

#### Test6: Harmonization of SDIP and PLANAR

Case1(positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LC | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | 0.6 | -0.5 | -0.2 | 0.5 | -0.1 | 0.3 |
| Class B | 0.7 | 0.2 | 0.2 | 0.5 | 0.4 | 0.4 |
| Class C | 0.3 | 0.0 | 0.0 | 0.4 | 0.3 | 0.3 |
| Class D | 0.4 | 0.0 | 0.0 | 0.4 | 0.4 | 0.4 |
| Class E | 0.8 | 0.1 | -0.2 | 0.7 | 0.3 | 0.3 |
| **All** | **0.6** | **0.0** | **0.0** | **0.5** | **0.2** | **0.3** |
| Enc Time[%] | 96% | | | 95% | | |
| Dec Time[%] | 100% | | | 100% | | |

Case2 (positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LC | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | 0.6 | -0.4 | -0.2 | 0.5 | 0.1 | 0.5 |
| Class B | 0.8 | 0.3 | 0.3 | 0.5 | 0.6 | 0.6 |
| Class C | 0.5 | 0.1 | 0.0 | 0.4 | 0.4 | 0.5 |
| Class D | 0.4 | 0.1 | 0.0 | 0.4 | 0.5 | 0.5 |
| Class E | 1.1 | 0.1 | 0.1 | 0.7 | 0.8 | 0.8 |
| **All** | **0.6** | **0.0** | **0.1** | **0.5** | **0.5** | **0.6** |
| Enc Time[%] | 98% | | | 97% | | |
| Dec Time[%] | 100% | | | 100% | | |

Case3:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LC | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | -0.1 | -0.2 | -0.3 | -0.1 | -0.2 | -0.2 |
| Class B | -0.1 | -0.2 | -0.2 | -0.1 | -0.1 | -0.1 |
| Class C | 0.0 | -0.1 | -0.1 | 0.0 | 0.0 | 0.0 |
| Class D | 0.0 | -0.1 | -0.1 | 0.0 | -0.1 | 0.0 |
| Class E | -0.2 | -0.5 | -0.4 | -0.2 | -0.3 | -0.1 |
| **All** | **-0.1** | **-0.2** | **-0.2** | **-0.1** | **-0.1** | **-0.1** |
| Enc Time[%] | 100% | | | 101% | | |
| Dec Time[%] | 100% | | | 101% | | |

#### Test7: Harmonization of SDIP and deblocking filter

**1: Tsinghua, HiSilicon test case**

Case 1:

Case2 (positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LC | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | -2.0 | 0.3 | 0.4 | 0.9 | 2.3 | 2.5 |
| Class B | -1.2 | 0.4 | 1.0 | 1.0 | 3.5 | 4.5 |
| Class C | -0.7 | 0.2 | 0.4 | 0.1 | 3.0 | 3.7 |
| Class D | -0.6 | 0.4 | 0.5 | 0.0 | 3.2 | 3.9 |
| Class E | -0.6 | 1.4 | 1.6 | 1.5 | 7.1 | 7.5 |
| **All** | **-1.1** | **0.5** | **0.8** | **0.7** | **3.6** | **4.3** |
| Enc Time[%] | 101% | | | 102% | | |
| Dec Time[%] | 95% | | | 90% | | |

Case3:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Intra | | | Intra LC | | |
| Y BD-rate | U BD-rate | V BD-rate | Y BD-rate | U BD-rate | V BD-rate |
| Class A | 0.08 | 0.01 | 0.00 | 0.09 | 0.01 | -0.01 |
| Class B | 0.15 | 0.05 | 0.05 | 0.17 | 0.03 | 0.04 |
| Class C | 0.05 | 0.01 | 0.01 | 0.04 | 0.00 | 0.02 |
| Class D | 0.07 | 0.00 | 0.00 | 0.11 | 0.00 | 0.00 |
| Class E | 0.26 | -0.04 | -0.05 | 0.20 | -0.15 | -0.12 |
| **All** | **0.12** | **0.01** | **0.01** | **0.12** | **-0.01** | **-0.01** |
| Enc Time[%] | 100% | | | 102% | | |
| Dec Time[%] | 100% | | | 102% | | |

**2: Qualcomm test case**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
|  | Y | U | V | Y | U | V |
| Class A | -0.07 | 0.00 | 0.00 | -0.09 | 0.01 | -0.01 |
| Class B | -0.02 | 0.05 | 0.05 | -0.07 | 0.03 | 0.03 |
| Class C | -0.14 | 0.00 | 0.00 | -0.19 | 0.00 | 0.02 |
| Class D | -0.09 | 0.00 | -0.01 | -0.10 | 0.00 | 0.00 |
| Class E | -0.06 | -0.06 | -0.06 | -0.16 | -0.15 | -0.12 |
| **Overall** | **-0.08** | **0.00** | **0.00** | **-0.12** | **-0.01** | **-0.01** |
| Enc Time[%] | 100% | | | 101% | | |
| Dec Time[%] | 100% | | | 101% | | |

#### Test8: Harmonization of SDIP and DC prediction filtering

Case1(positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | 0.10 | 0.04 | 0.14 | 0.15 | 0.21 | 0.28 |
| Class B | 0.13 | 0.06 | 0.02 | 0.17 | 0.15 | 0.15 |
| Class C | 0.11 | 0.11 | 0.13 | 0.14 | 0.19 | 0.11 |
| Class D | 0.08 | 0.08 | 0.10 | 0.12 | 0.19 | 0.14 |
| Class E | 0.03 | 0.03 | 0.07 | 0.11 | 0.03 | 0.03 |
| **Overall** | **0.09** | **0.06** | **0.09** | **0.14** | **0.16** | **0.15** |
| Enc Time[%] | 102% | | | 99% | | |
| Dec Time[%] | 100% | | | 100% | | |

Case 2 (positive means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | 0.12 | 0.07 | 0.22 | 0.18 | 0.23 | 0.36 |
| Class B | 0.18 | 0.08 | 0.08 | 0.21 | 0.18 | 0.20 |
| Class C | 0.19 | 0.14 | 0.15 | 0.21 | 0.20 | 0.19 |
| Class D | 0.13 | 0.13 | 0.10 | 0.17 | 0.13 | 0.16 |
| Class E | 0.08 | 0.02 | 0.05 | 0.17 | 0.11 | 0.10 |
| **Overall** | **0.15** | **0.09** | **0.12** | **0.19** | **0.17** | **0.21** |
| Enc Time[%] | 107% | | | 102% | | |
| Dec Time[%] | 100% | | | 99% | | |

### Cross verification status and proponents

#### Test1: Harmonization of SDIP and RQT

Proponents: Tsinghua, USTC, HiSilicon, Microsoft, Huawei

|  |  |  |
| --- | --- | --- |
| **Cross-checker** | **Case 1: RQT syntax harmonization** | **Case2: two depth RQT of 8x32/32x8** |
| Sony | match | match |
|  |  |  |
|  |  |  |

#### Test2: Harmonization of SDIP and Mode-Dependent DCT/DST

Proponents: Huawei, HiSilicon

|  |  |  |  |
| --- | --- | --- | --- |
| **Cross-checker** | **SDIP = 0** | **SDIP = 1** | |
| **MDDT=0**  **Case 1** | **MDDT=0**  **Case 2** | **MDDT=1&SDIP\_MDDT=1**  **Case3** |
| TI |  |  |  |
| BBC |  | match |  |
| NEC |  | match |  |
| Orange Labs. | match |  |  |

#### Test3: Harmonization of SDIP and MDCS

Proponent: Microsoft

|  |  |
| --- | --- |
| **Cross-checker** | **SDIP = 1** |
| **MDCS=1&SDIP\_MDCS=0** |
| Sony | match |
| NEC | match |
| INRIA | match |

#### Test4: Harmonization of LM mode and the chroma prediction in SDIP

Proponents: LGE, Microsoft

|  |  |  |
| --- | --- | --- |
| **Cross-checker** | **SDIP=1** | |
| **Case1(LG)** | **Case2(Microsoft)** |
| Sharp | match |  |

#### Test5: Harmonization of SDIP and MDIS

1. **Proponents: Santa Clara University University, HiSilicon**

|  |  |  |  |
| --- | --- | --- | --- |
| **Cross-checker** | **SDIP=0** | **SDIP = 1** | |
| **MDIS=0**  **Case1** | **MDIS=0**  **Case2** | **MDIS=1&SDIP\_MDIS=1**  **Case3** |
| Qualcomm | match | match |  |
| NEC |  |  | match |

1. **Qualcomm test case**

|  |  |
| --- | --- |
| **Cross-checker** | Qualcomm test case |
| Ghent University | match |

#### Test6: Harmonization of SDIP and PLANAR

Proponents: HiSilicon, Tsinghua

|  |  |  |  |
| --- | --- | --- | --- |
| **Cross-checker** | **SDIP=0** | **SDIP = 1** | |
| **PLANAR =0**  **Case1** | **PLANAR =0**  **Case2** | **PLANAR =1&SDIP\_ PLANAR =1**  **Case3** |
| Canon | match | match | match |

#### Test7: Harmonization of SDIP and deblocking filter

1. **Proponents: Tsinghua, HiSilicon**

|  |  |  |  |
| --- | --- | --- | --- |
| **Cross-checker** | **SDIP=0** | **SDIP = 1** | |
| deblocking filter **=0**  **case1** | deblocking filter **=0**  **case2** | deblocking filter **=1&SDIP\_** deblocking filter **=1**  **case3** |
| Qualcomm |  | match |  |
| NEC |  | match | match |

1. **Proponents: Qualcomm**

|  |  |
| --- | --- |
| **Cross-checker** | **QCSDIPDB** |
| Mediatek |  |

#### Test8: Harmonization of SDIP and DC prediction filtering

Proponent: Qualcomm

|  |  |  |
| --- | --- | --- |
| **Cross-checker** | **SDIP=0, DC prediction filter = 0** | **SDIP=1, DC prediction filter = 0** |
| HiSilicon |  |  |

## CE6.c: Differential Coding of Intra Modes (DCIM) JCTVC-E318

DCIM (Differential Coding of Intra Modes) is a method categorized as Edge based Intra Prediction, which has been evaluated in the past CE [1]. The latest DCIM results are summarized in JCTVC-E318 [2]. In this experiment, the performance of DCIM on the latest reference software i.e., HM3.0 is evaluated.

Case 1: DCIM default (negative means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | -0.2 | 0.0 | 0.1 | -0.2 | 0.0 | 0.0 |
| Class B | -0.7 | -1.0 | -1.1 | -0.5 | -0.4 | -0.5 |
| Class C | -1.2 | -1.1 | -1.1 | -1.4 | -0.7 | -0.8 |
| Class D | -0.7 | -0.4 | -0.4 | -0.6 | -0.1 | -0.2 |
| Class E | -1.0 | -1.3 | -0.9 | -0.8 | -1.0 | -0.7 |
| **Overall** | **-0.8** | **-0.7** | **-0.7** | **-0.7** | **-0.4** | **-0.5** |
| Enc Time[%] | 113% | | | 124% | | |
| Dec Time[%] | 103% | | | 105% | | |

Case 2: DCIM with subdirection off (negative means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | -0.1 | 0.3 | 0.3 | 0.0 | 0.2 | 0.2 |
| Class B | -0.3 | -0.3 | -0.2 | -0.1 | 0.0 | 0.0 |
| Class C | -0.8 | -0.5 | -0.5 | -1.1 | -0.3 | -0.4 |
| Class D | -0.6 | -0.2 | -0.2 | -0.6 | -0.1 | -0.1 |
| Class E | -0.3 | -0.1 | 0.1 | -0.1 | -0.3 | -0.1 |
| **Overall** | **-0.4** | **-0.2** | **-0.1** | **-0.4** | **-0.1** | **-0.1** |
| Enc Time[%] | 106% | | | 114% | | |
| Dec Time[%] | 103% | | | 106% | | |

Case 3: DCIM with BIP off (negative means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | -0.2 | 0.1 | 0.0 | -0.1 | 0.1 | 0.1 |
| Class B | -0.7 | -1.0 | -1.2 | -0.4 | -0.3 | -0.5 |
| Class C | -1.1 | -1.1 | -1.0 | -1.2 | -0.5 | -0.6 |
| Class D | -0.6 | -0.4 | -0.4 | -0.4 | -0.1 | -0.1 |
| Class E | -1.0 | -1.2 | -0.8 | -0.6 | -0.9 | -0.7 |
| **Overall** | **-0.7** | **-0.7** | **-0.7** | **-0.5** | **-0.3** | **-0.3** |
| Enc Time[%] | 110% | | | 119% | | |
| Dec Time[%] | 103% | | | 104% | | |

Case 4: DCIM with 4TAP off (negative means gain here):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | All Intra HE | | | All Intra LC | | |
| Y | U | V | Y | U | V |
| Class A | -0.2 | 0.2 | 0.1 | -0.2 | 0.0 | 0.0 |
| Class B | -0.3 | -0.6 | -0.7 | 0.1 | 0.1 | 0.0 |
| Class C | -0.6 | -0.5 | -0.4 | -0.5 | -0.1 | -0.1 |
| Class D | -0.3 | 0.1 | 0.1 | 0.0 | 0.3 | 0.2 |
| Class E | -0.4 | -0.8 | -0.3 | 0.1 | -0.4 | -0.1 |
| **Overall** | **-0.4** | **-0.3** | **-0.3** | **-0.1** | **0.0** | **0.0** |
| Enc Time[%] | 111% | | | 121% | | |
| Dec Time[%] | 103% | | | 105% | | |

## CE6.d: Parallel Intra Coding

In contribution (JCTVC-E315), the concept of parallel intra-prediction unit (PPU) is introduced. The PPU defines the size of a block that can be coded using parallelization. The motivation is to increase the degree of parallelism for small blocks sizes. The blocks within the PPU are divided into two sets, and blocks within each set are predicted in parallel. The second set of blocks depend on the first set of blocks. For more information, see JCTVC-E315.

In this sub-CE, we will test the coding efficiency degradation of the JCTVC-E315 with different definitions for the first and second set blocks. (Including, a checker board assignment and a vertical assignment.) Additionally, we will consider the case of disabling 4x4 predictions completely as a second point of reference.

## CE6.e: Intra Smoothing

### JCTVC-D282:”Adaptive intra smoothing”, Qualcomm

In this proposal, an adaptive intra smoothing method is proposed. Multiple filters are introduced and investigated in order to improve the performance of the current intra smoothing method in HM3.0. Filter modes are explicitly and implicitly signaled.

### JCTVC-E437: “On intra coding and MDIS”, Sharp

This proposal seeks to improve the mode dependent intra smoothing (MDIS) technique that was adopted in the previous meeting. MDIS filters the source pixels used for intra prediction with different degrees of smoothing, with the degree determined by the intra prediction direction. The document reports that using edge directed smoothing in the construction of the neighborhood mitigates these issues. For a detailed description of the method see JCTVC-E437.