



JCTVC-E054: Preliminary complexity assessment on ARM

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Problem statement

- HM complexity assessment is typically conducted on PC platforms → Intel Architecture is implicitly selected as reference architecture.
- Considering the current multimedia market status, ARM architecture is relevant.

ST-Ericsson U8500

- Purpose: HM 2.0 complexity assessment on ARM architecture.
- Platform: experimental board of ST-Ericsson U8500, with Dual Cortex-A9 CPU.
- Comparison with PC platform.

	U8500	PC
CPU	ARM Dual Cortex-A9	Intel Core 2 Duo P8600
Frequency	450 MHz	2.40 GHz
Physical memory	200 MB	2 GB
Swap memory	0	2 GB
OS	Linux (2.6.29)	Cygwin_NT-5.1
g++ version	4.4.1	4.3.4



- HM 2.0 decoding time measured on “Low Delay” anchor bitstreams.
- Ratio between “High Efficiency” and “Low Complexity” configurations is reported.

	Intel	ARM
Min	1.16	1.12
Average	1.77	1.60
Max	2.23	2.10

- Notes
 1. The board could not decode streams at 1920x1080 spatial resolution because of excessive memory requirements.
 2. The board could not decode “Vidyo4” streams in LD-HE configuration with QP 32 and 37.

Conclusions

- ARM CPU architecture is relevant for HEVC complexity assessment.
- In the scope of the Complexity Assessment AHG, it is proposed to:
 - Conduct further complexity experiments on ARM
 - Compare to results obtained on PC platforms
 - Report the results at next JCT-VC meetings

References

- D.Alfonso, “*Proposals for video coding complexity assessment*”, JCTVC-B020, 2nd JCT-VC meeting, July 2010, Geneva, CH.
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<http://www.stericsson.com/platforms/U8500.jsp>
- ARM Cortex™-A9 Processor,
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