AhG Report:
Spatial Transforms

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Spatial Transforms AhG

- Formed in Guangzhou

- Chair: Pankaj Topiwala, FastVDO

  - Vice-Chairs:

    - Robert Cohen, Mitsubishi

    - Madhukar Budagavi, TI

    - Rajan Joshi, Qualcomm

Mandate

- Study the transforms in the HM design, including compression performance, computational complexity, dynamic range, storage requirements, etc.

- Perform analysis of block transform design and architecture, including software and hardware considerations.

- Discuss transform-related Core Experiments, and identify potential synergies or incompatibilities related to the tools being tested in the CEs.

- Report the results and conclusions of these discussions and experiments to the JCT-VC.

Since Guangzhou

- Active reflector

  - Some 20 reflector emails

  - And non-reflector dialog

  - Interest in advancing designs, complexity measures

  - Numerous contributions

    - Alt transforms
    - Core transforms
    - Complexity-related

Two Areas

- Core Transforms
  - Basic 4-pt to 32-pt transforms, approx. DCTs
  - Seek complexity reduction without perf. loss
- Alternative Transforms, CE7
  - Transforms specific to intra-coding (ROT, MDDT..)
  - Seek performance gain without high complexity

Core Transform Proposals

Spatial Transforms AhG Docs

Doc	Source	Authors	Brief Title
D036	TI	M. Sadafale, M. Budagavi	Matrix multiplication spec for HeVC
D037	TI	M. Budagavi, A. Gupte	DCT+Hadamard large transforms
D071	Sharp	K. Misra et al	On transform dynamic range
D224	Cisco	G. Bjontegaard et al	Unified Transforms w/ 16-bit data rep.
D256	Qualcomm	R. Joshi et al	Efficient 16 and 32-pt transforms
D257	Qualcomm	J. Sole et al	32-pt with partial freq transform
D339	FastVDO	W. Dai et al	Fast, Mult-Free Transforms for HM
D365	Samsung/FastVDO	Y. Hong et al	Fast Int Transforms, Complexity Analysis

Topic Areas

- Fast, integer transforms, perf. matches HM
- Low arithmetic complexity (mults, adds, shifts)
- Or convenience of execution (matrix mult.)
- Memory storage and bandwidth considerations
- Dynamic range considerations
  - i.e., 16-pt and 32-pt arithmetic not the same
- Special large transforms
  - Partial frequency (32-pt, keep low-freq components)
  - 16-pt x H2 (Hadamard) for 32-pt

Alt Transforms Proposals

Proponent (Tool Type)	CE7 Doc.	Cross-verification			Other related docs.
Toshiba (1DDUT)	D107	D264 (Qualcomm)	D032 (Samsung)		
I^2R (DCT/Derived KLT-DST)	D046	D353 (Samsung)	D306 (Huawei)	D104 (Toshiba)	D048 D049
Samsung (Fast ROT)	D357	D030 (MERL)	D409 (Qualcomm)	DXXX (Mediatek)	D180
Samsung (DCT/DST)	D033	D105 (Toshiba)	D031 (BBC)	D088 (NHK)	
Qualcomm (MDDT Improvements)	D399	D307 (Huawei)	D354 (Samsung)	D078 (I^2R)	D392
Huawei (Symmetry-based MDDT simplification)	D304	D047 (I^2R)			
Peking Univ. (Residual reordering)	D284	D290 (Mediatek)			D286

Topic Areas

- Transforms for Intra Coding
    - Fast ROT
    - MDDT Simplifications
    - Other related transforms

Complexity Analysis

Dimensions of Complexity

Arithmetic Operations (mults, adds, shifts)

Memory and Memory Bandwidth

Dynamic Range Analysis

 - Bitwidth of data registers

 - Bitwidth of accumulators/ALUs

Throughput

Work Plan for Meeting

- Review proposals and cross-checks

- Discuss tradeoffs in performance vs complexity (in several dimensions) of proposed designs

- Develop consensus on recommendations

- Propose relevant CEs; likely

    - Continue Alt Trans CE7

    - Add CE on Core Transform Architectures

- Initial meeting tonight after JCTVC, tbd