

TE8: TI Parallel context processing (PCP) proposal (JCTVC-B062.doc)

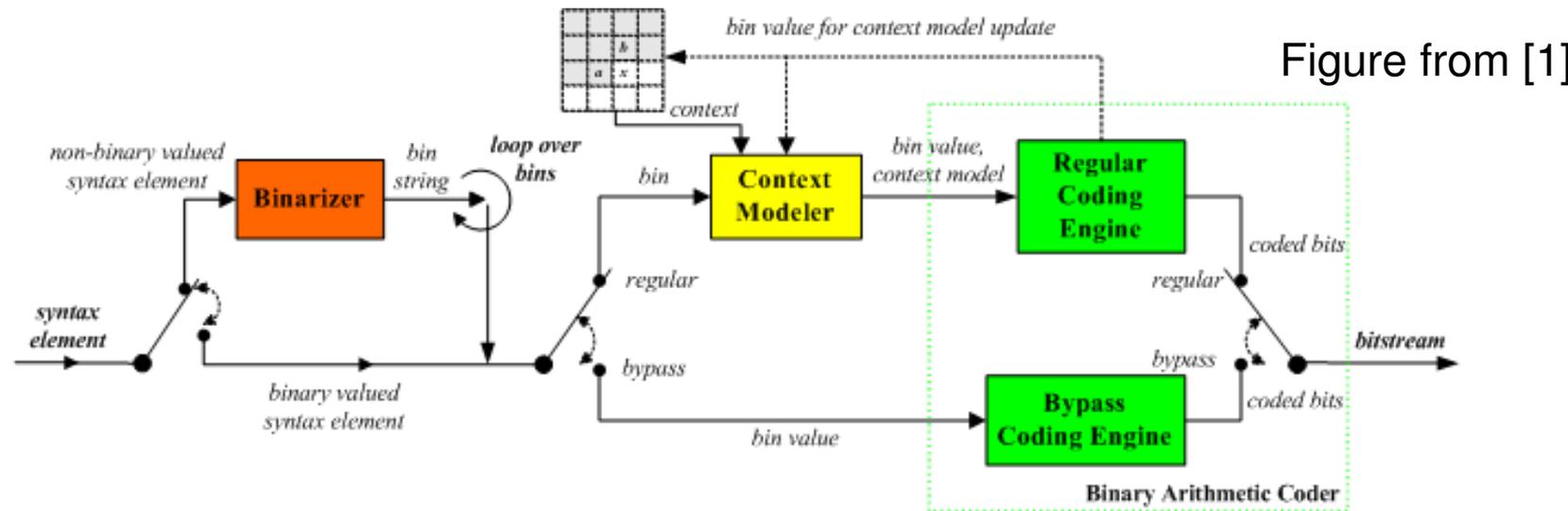
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of ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11
3rd Meeting: Guangzhou, CN, 7-15 October, 2010**



Motivation



- CABAC is a highly serial processing block
- Serial nature comes from:
 - Binarizer (variable length coding)
 - Context modeler (probability depends on LPS/MPS, position of bin)
 - Binary arithmetic coder (interval subdivision)

Parallel Context Processing (PCP)

- Simple data rearrangement techniques within a block to enable parallelization of context processing
- Three types of PCP proposed
 - Coeff Level BinIdx 0 PCP
 - Coefficient Sign PCP
 - Significance Map PCP
- Techniques applicable to all high-efficiency entropy coding options
 - CABAC, PIPE/V2V etc.

Coeff sign PCP

AVC coding of coefficient levels and sign

```
for (i = MaxNumCoeff(BlockType)-1; i >= 0; i--)  
{  
  {  
    Encode coeff_abs_level_minus1[i];  
    Encode coeff_sign_flag[i];  
  }  
}
```

Coefficient sign PCP: Code sign in a different plane

```
for (i = MaxNumCoeff(BlockType)-1; i >= 0; i--)  
{  
  Encode coeff_sign_flag[i];  
}  
  
for (i = MaxNumCoeff(BlockType)-1; i >= 0; i--)  
{  
  Encode coeff_abs_level_minus1[i];  
}
```

Coeff Level BinIdx 0 PCP

- Coeff Level BinIdx 0 PCP technique codes BinIdx 0 in a different plane
- Context (ctxIdxInc) used for `coeff_abs_level_minus1` depends on the position of the bin (binIdx) in AVC

If binIdx is equal to 0, ctxIdxInc is derived by

$$\text{ctxIdxInc} = ((\text{numDecodAbsLevelGt1} \neq 0) ? 0 : \text{Min}(4, 1 + \text{numDecodAbsLevelEq1})) \quad (9-23)$$

Otherwise (binIdx is greater than 0), ctxIdxInc is derived by

$$\text{ctxIdxInc} = 5 + \text{Min}(4 - ((\text{ctxBlockCat} == 3) ? 1 : 0), \text{numDecodAbsLevelGt1}) \quad (9-24)$$

- Context processing for all the bins with binIdx 0 for all the coeffs level in a block can be carried out in parallel to bin processing of binIdx = 0 and before the decoding of bins with binIdx != 0

Coeff sign PCP and Coeff Level BinIdx 0 PCP

	Intra - TI-PCP-Run1 (Sign&Bin0)		
	Y BD- rate	U BD- rate	V BD- rate
Class A	0.0	0.0	0.0
Class B	0.0	0.0	0.0
Class C	0.0	0.0	0.0
Class D	0.0	0.0	0.0
Class E	0.0	0.0	0.0
All	0.0	0.0	0.0
Avg speedup factor	2.6		
Max speedup factor	3.0		

Thanks for MediaTek for cross-checking proposal

Coeff sign PCP and Coeff Level BinIdx 0 PCP

	Random access - TI-PCP-Run1 (Sign&Bin0)		
	Y BD-rate	U BD-rate	V BD-rate
Class A	0.0	0.1	0.1
Class B	0.0	-0.1	-0.1
Class C	0.0	-0.1	0.0
Class D	0.0	-0.1	0.0
Class E			
All	0.0	-0.1	0.0
Avg speedup factor	2.6		
Max speedup factor	3.0		

Thanks for MediaTek for cross-checking proposal

Coeff sign PCP and Coeff Level BinIdx 0 PCP

	Low delay - TI-PCP-Run1 (Sign&Bin0)		
	Y BD-rate	U BD-rate	V BD-rate
Class A			
Class B	0.0	0.1	0.2
Class C	0.0	-0.1	0.1
Class D	0.0	0.0	0.2
Class E	0.0	0.2	0.5
All	0.0	0.1	0.2
Avg speedup factor	2.2		
Max speedup factor	3.0		

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Significance Map PCP (1)

AVC significance map coding

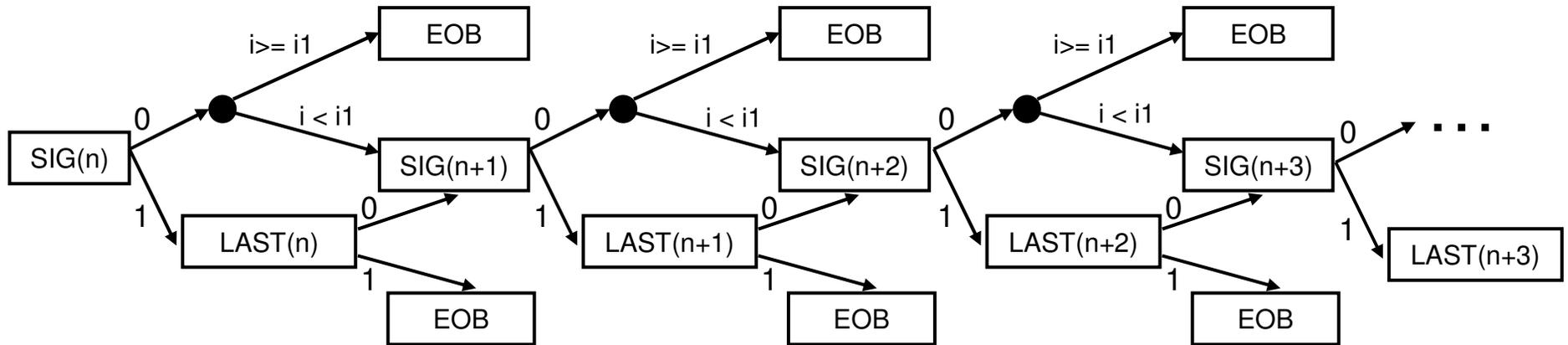
```
for (i = 0 ;i < MaxNumCoeff(BlockType)-1 ;i++)
{
    Encode significant_coeff_flag[i];
    if(significant_coeff_flag[i])
        Encode last_significant_coeff_flag[i];
    if (last_significant_coeff_flag[i])
        break ;
}
```

Significance Map PCP (2)

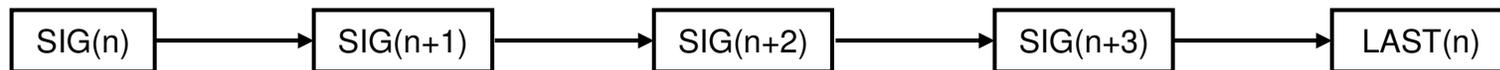
Significance map PCP – Code one last every K significant_coeff_flag

```
for (i = 0 ;i < MaxNumCoeff(BlockType)-1 ;i += K)
{
    if(i+K < MaxNumCoeff(BlockType)-1)
        j1 = K ;
    else
        j1 = K-1 ;
    sig = 0 ;
    for (j = 0 ;j < j1 ;j++)
    {
        Encode significant_coeff_flag[i*K+j];
        sig += significant_coeff_flag[i*K+j]
    }
    if(sig)
        Encode last_significant_coeff_flag[i];
    if (last_significant_coeff_flag[i])
        break ;
}
```

Significance map PCP (3)



(a) 5X parallelism in AVC CABAC SigMap context processing using speculative computing (which happens every bin). Counter i indicates bin position, $i1$ is $\text{MaxNumCoeff}(\text{BlockType})-1$, EOB denotes end of block. SIG - significant_coeff_flag. LAST - last_significant_coeff_flag.



(b) 5X parallelism in "N SIG, 1 LAST" context processing using speculative computing (which happens at only 5th bin).

Significance map PCP (4)

- Last every 2 Sigmap (2SIG1L) was implemented in TMuC-0.7
 - HHI_TRANSFORM_CODING was disabled
 - There is net bin savings due to reduction in number of total bins for some configurations
 - Note number of sig map bins increases but number of last decreases
 - About 4X savings in number contexts that need to be fetched for 3X parallelism

Significance map PCP

	Intra - TI-PCP-Run2 (Sigmap PCP)		
	Y BD-rate	U BD-rate	V BD-rate
Class A	0.4	1.6	1.6
Class B	0.3	1.4	1.5
Class C	0.2	1.7	1.6
Class D	0.2	1.4	1.5
Class E	0.7	1.1	1.5
All	0.3	1.5	1.5
Avg speedup factor due to reduction of bins	1.1		
Max speedup factor due to reduction of bins	1.2		
Parallelism	3X		

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Significance map PCP

	Random access - TI-PCP-Run2 (Sigmap PCP)		
	Y BD-rate	U BD-rate	V BD-rate
Class A	0.2	1.0	0.8
Class B	0.1	1.1	1.0
Class C	0.0	1.0	1.0
Class D	0.1	0.7	0.5
Class E			
All	0.1	1.0	0.8
Avg speedup factor due to reduction of bins	1.1		
Max speedup factor due to reduction of bins	1.3		
Parallelism	3X		

Thanks for RIM for cross-checking proposal

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Significance map PCP

	Low delay - TI-PCP-Run2 (Sigmap PCP)		
	Y BD-rate	U BD-rate	V BD-rate
Class A			
Class B	-0.1	1.4	1.7
Class C	-0.1	0.7	1.0
Class D	-0.1	1.5	1.4
Class E	0.1	3.4	2.1
All	-0.1	1.6	1.5
Avg speedup factor due to reduction of bins	1.0		
Max speedup factor due to reduction of bins	1.2		
Parallelism	3X		

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Conclusions

- Coefficient sign PCP and Coeff Level BinIdx 0 PCP tools
 - Provide a 2.6X to 3X speed up in context processing of coefficient sign and levels with no coding loss
 - Recommend that both these techniques be adopted into TMuC and TM
- Sigmap PCP tool
 - Used with `HHI_TRANSFORM_CODING = 0`
 - Reduces the number of bins generated by about 10% for Intra and Random access configurations
 - No reduction in number of bins generated for Low Delay configuration
 - Sigmap PCP reduces number of context that need to be speculatively fetched for parallel processing
 - Factor of 4X reduction in the worst case number of contexts that need to be speculatively fetched for achieving 3X parallelism with 2SIG1L Sigmap PCP
 - Recommend further study in Tool/Core experiment